FIG. 1

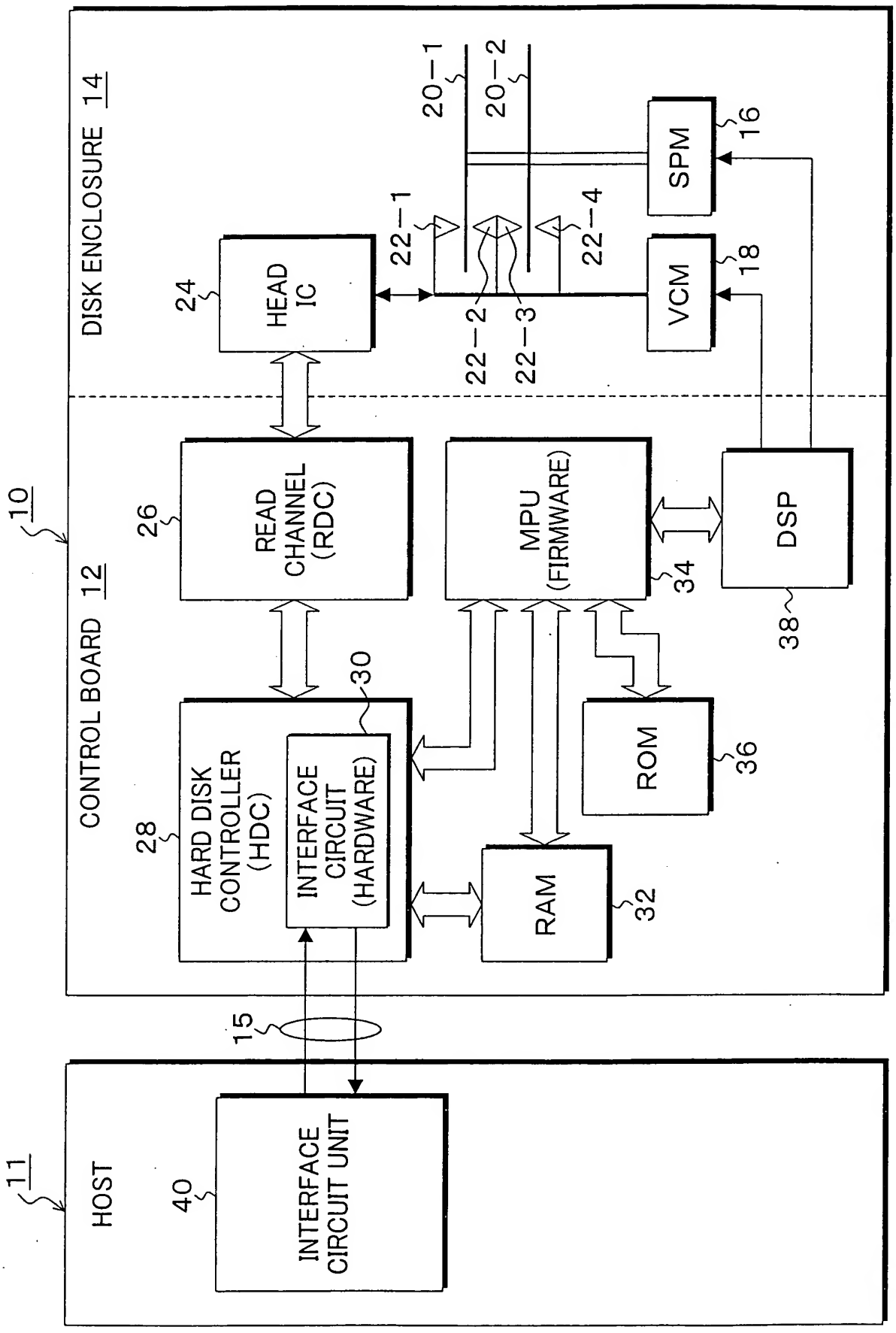

10
DISK ENCLOSURE 14
CONTROL BOARD 12
11
HOST
15
20—1
20—2
22—1
22—2
22—3
22—4
24
HEAD IC
SPM
16
VCM
18
26
READ CHANNEL (RDC)
MPU (FIRMWARE)
34
DSP
38
28
HARD DISK CONTROLLER (HDC)
30
INTERFACE CIRCUIT (HARDWARE)
ROM
36
RAM
32
40
INTERFACE CIRCUIT UNIT

FIG. 2

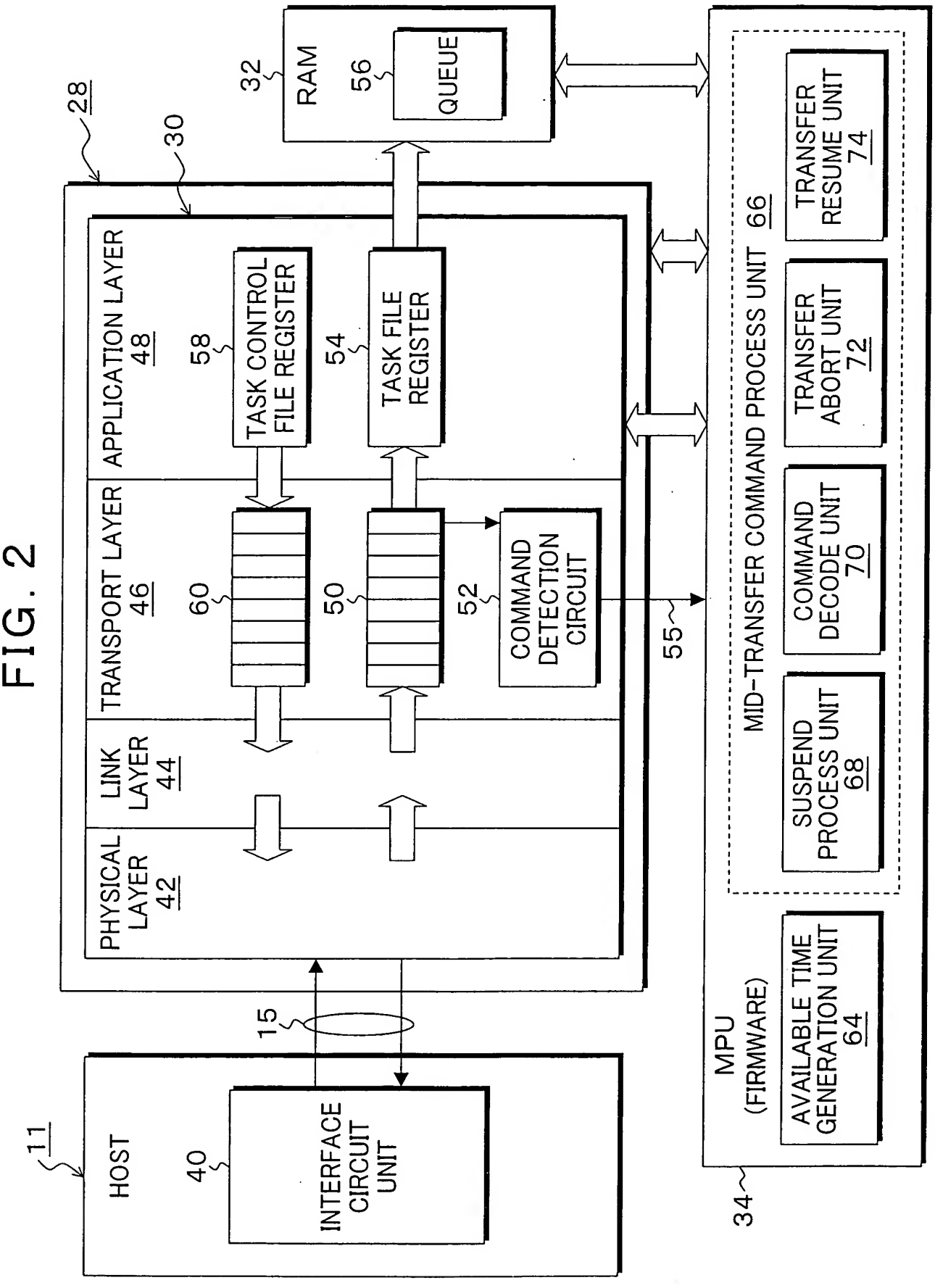

HOST
11
INTERFACE CIRCUIT UNIT
40
15
28
30
RAM
32
QUEUE
56
APPLICATION LAYER
48
TRANSPORT LAYER
46
LINK LAYER
44
PHYSICAL LAYER
42
TASK CONTROL FILE REGISTER
58
TASK FILE REGISTER
54
60
50
52
COMMAND DETECTION CIRCUIT
55
MPU
(FIRMWARE)
34
MID-TRANSFER COMMAND PROCESS UNIT
66
AVAILABLE TIME GENERATION UNIT
64
SUSPEND PROCESS UNIT
68
COMMAND DECODE UNIT
70
TRANSFER ABORT UNIT
72
TRANSFER RESUME UNIT
74

FIG. 3A

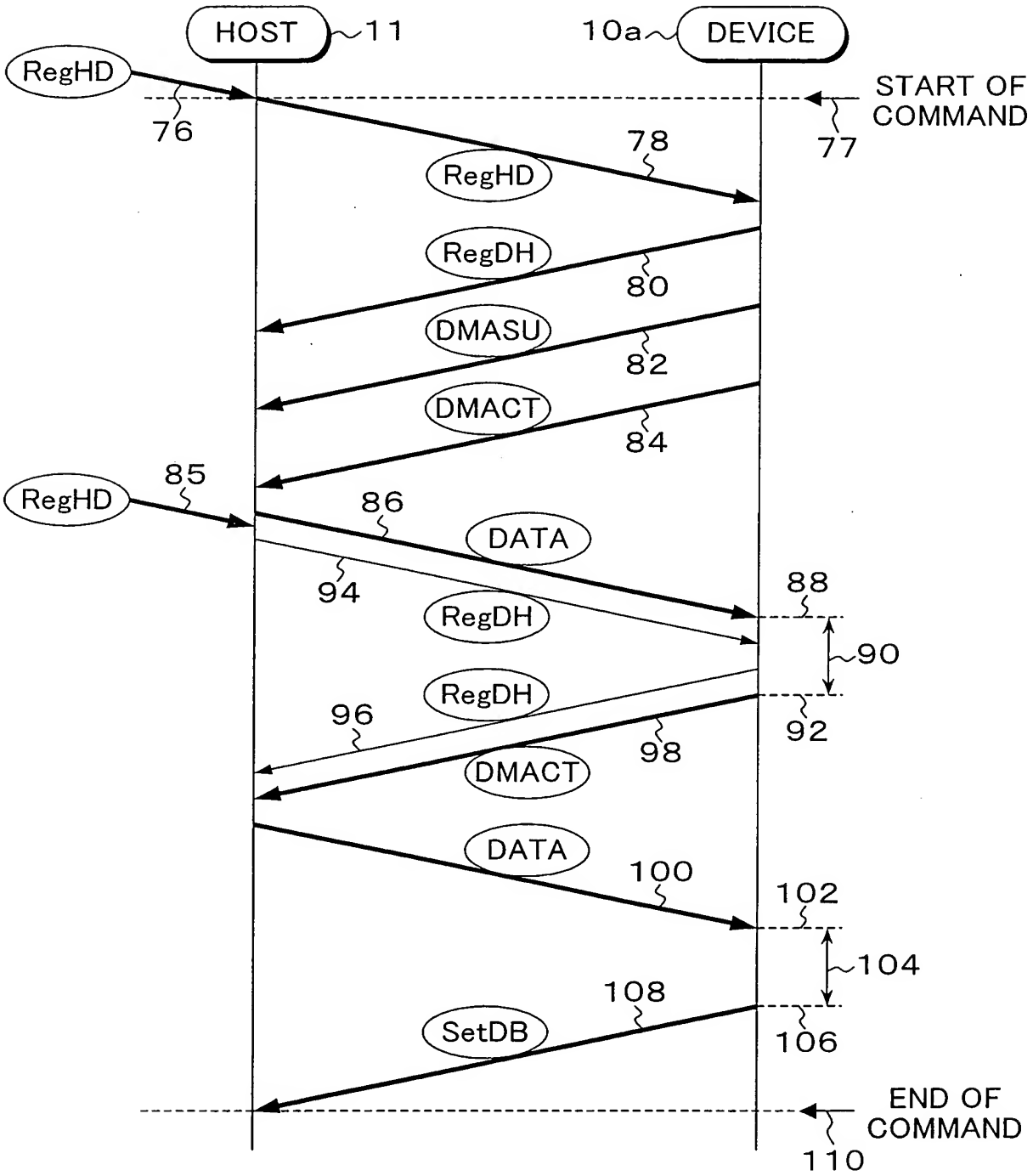

HOST
11
10a
DEVICE
RegHD
76
START OF COMMAND
77
78
RegHD
RegDH
80
DMASU
82
DMACT
84
85
RegHD
86
DATA
94
88
RegDH
90
RegDH
96
92
98
DMACT
DATA
100
102
104
108
SetDB
106
END OF COMMAND
110

FIG. 3B

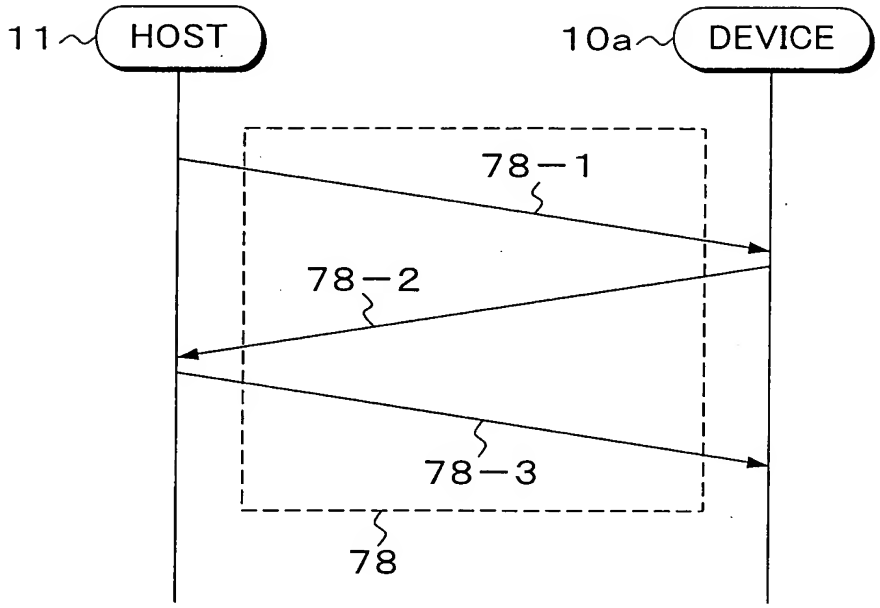


FIG. 4

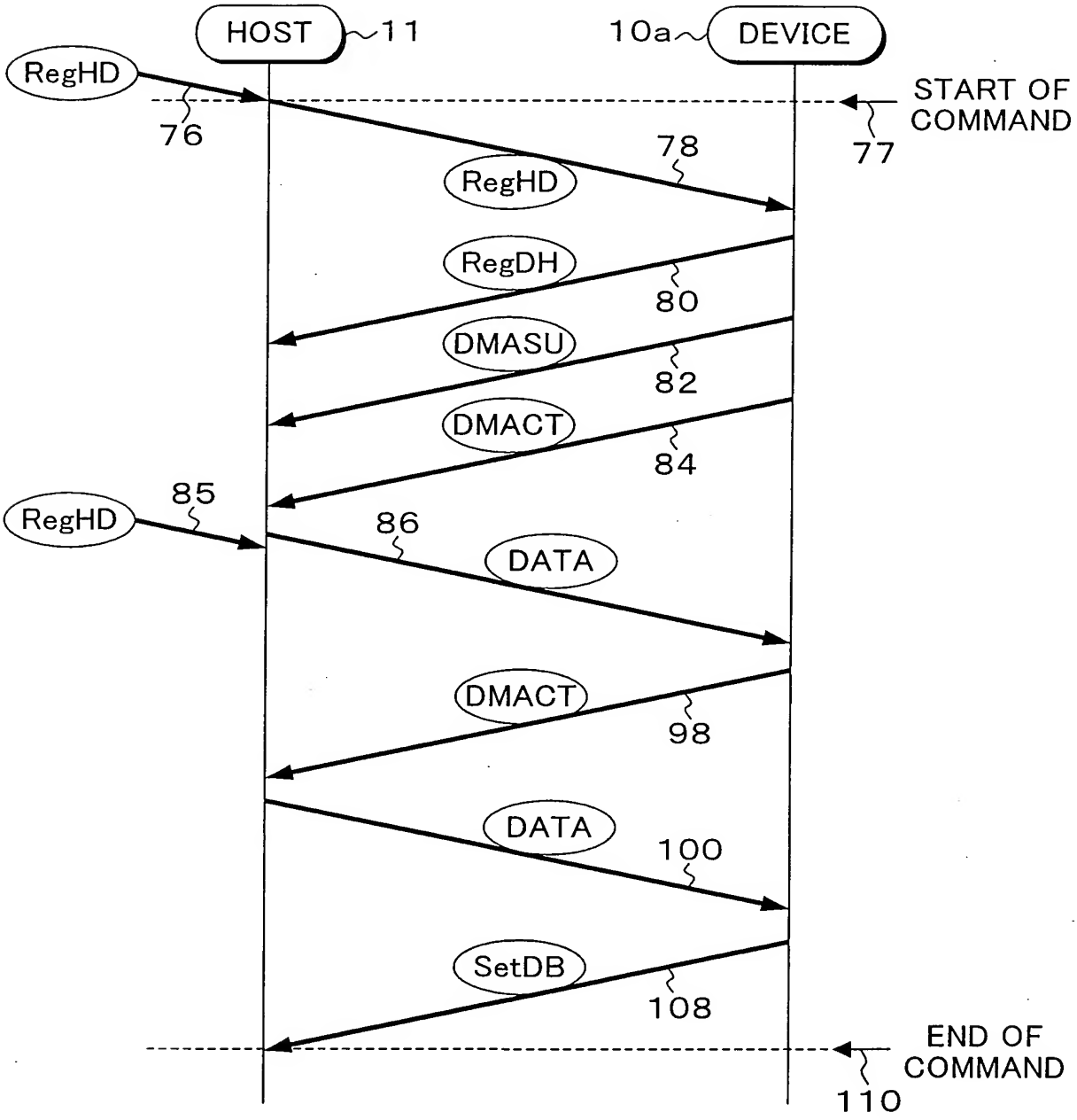
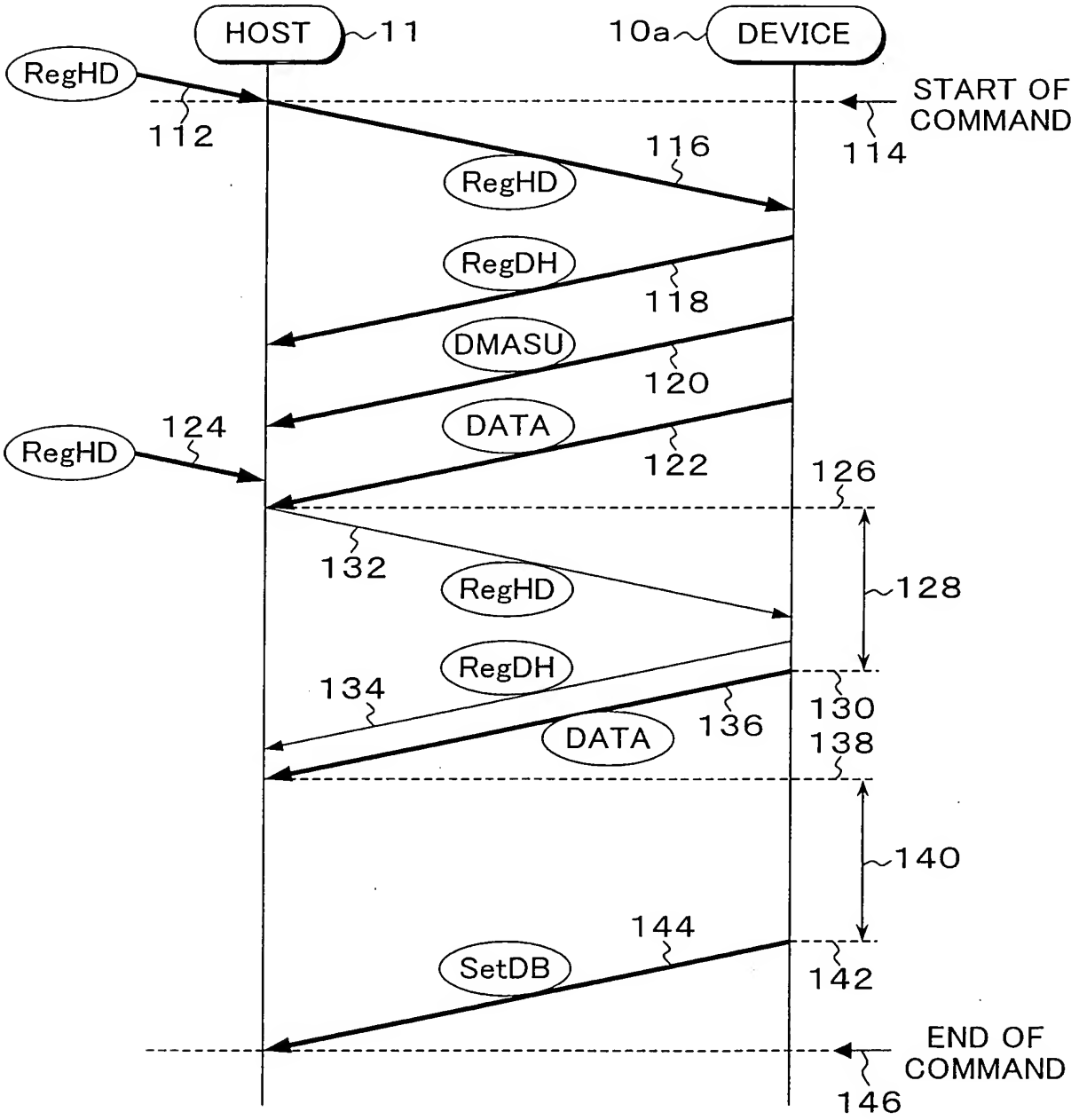

HOST
11
10a
DEVICE
RegHD
76
START OF COMMAND
77
78
RegHD
RegDH
80
DMASU
82
DMACT
84
85
RegHD
86
DATA
DMACT
98
DATA
100
SetDB
108
END OF COMMAND
110

FIG. 5


HOST
11
10a
DEVICE
RegHD
112
START OF COMMAND
114
116
RegHD
RegDH
118
DMASU
120
DATA
122
124
RegHD
126
132
RegHD
128
RegDH
134
130
DATA
136
138
140
144
SetDB
142
END OF COMMAND
146

PRIOR ART

FIG. 6

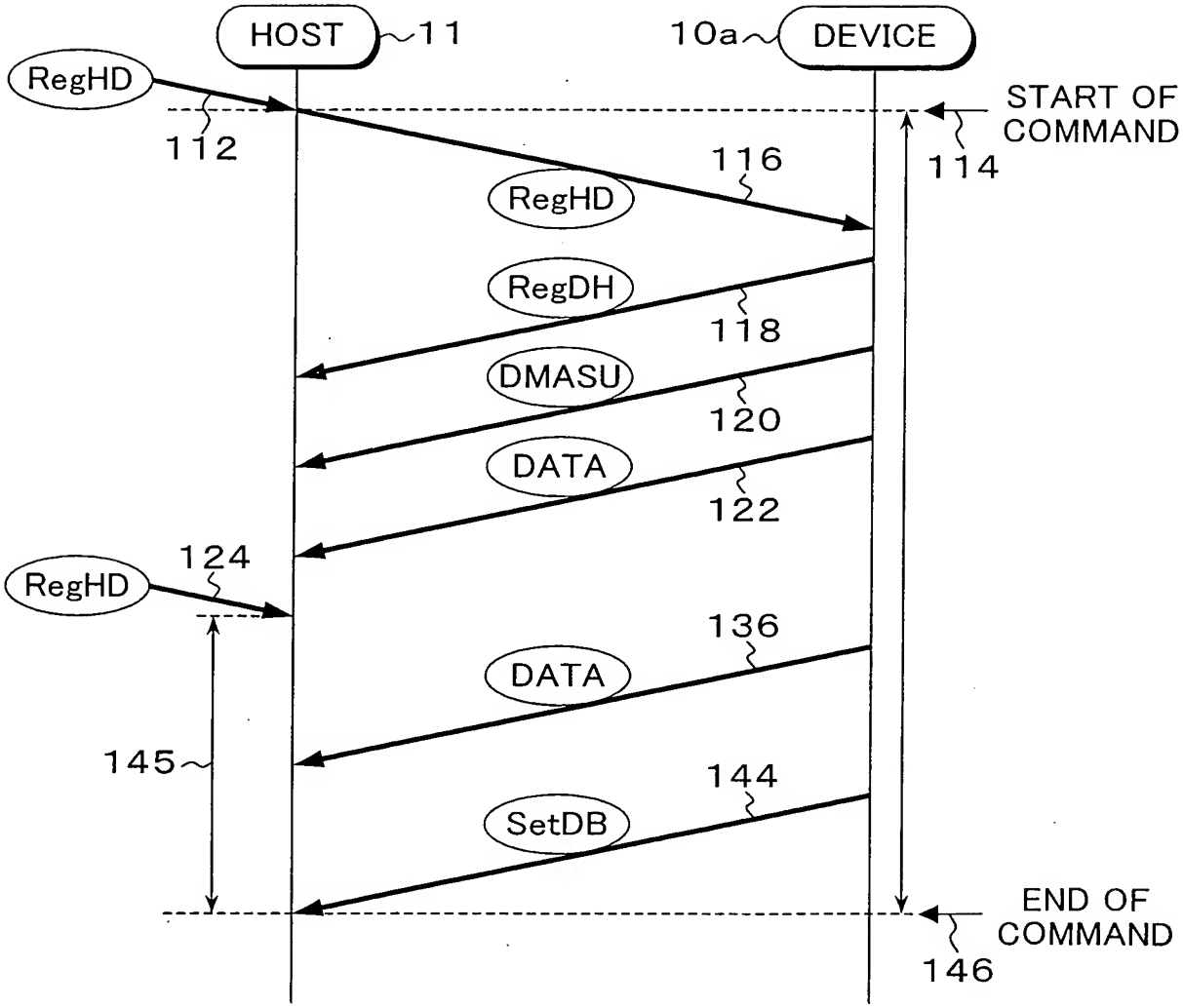


FIG. 7

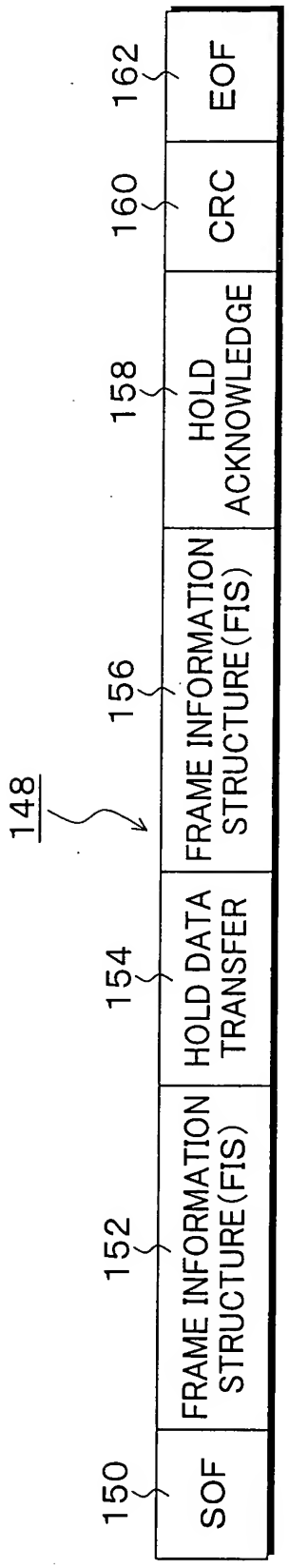

148
150
SOF
152
FRAME INFORMATION STRUCTURE(FIS)
154
HOLD DATA TRANSFER
156
FRAME INFORMATION STRUCTURE(FIS)
158
HOLD ACKNOWLEDGE
160
CRC
162
EOF

FIG. 8

164

	0	1	2	3	4
0	Features	Command	C	R	R	Reserved(0)	FIS Type(27h)
1	Dev/Head	Cyl High	Cyl Low				Sector Number
2	Features(exp)	Cyl High(exp)	Cyl Low(exp)				Sector Num(exp)
3	Control	Reserved(0)	Sector Count(exp)				Sector Count
4	Reserved(0)	Reserved(0)	Reserved(0)				Reserved(0)

FIG. 9

166

0	Error	Status	R	I	R	Reserved(0)	FIS Type(34h)
1	Dev/Head	Cyl High	Cyl Low				Sector Number
2	Reserved(0)	Cyl High(exp)	Cyl Low(exp)				Sector Num(exp)(0)
3	Reserved(0)	Reserved(0)	Sector Count(exp)				Sector Count
4	Reserved(0)	Reserved(0)	Reserved(0)				Reserved(0)

FIG. 10

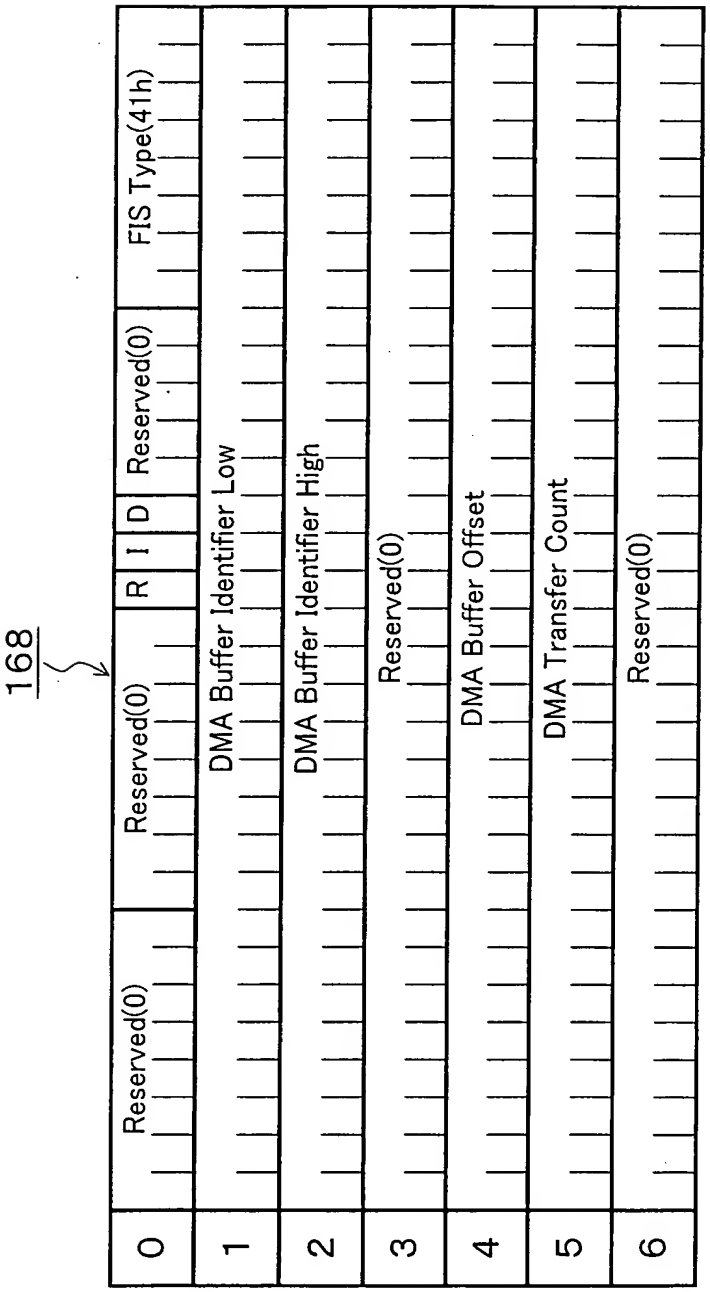

168
0
1
2
3
4
5
6
Reserved(0)
Reserved(0)
R
I
D
Reserved(0)
FIS Type(41h)
DMA Buffer Identifier Low
DMA Buffer Identifier High
Reserved(0)
DMA Buffer Offset
DMA Transfer Count
Reserved(0)

FIG. 11

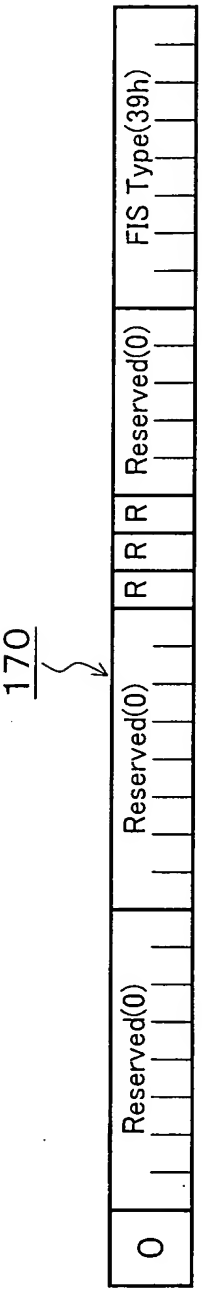


FIG. 12

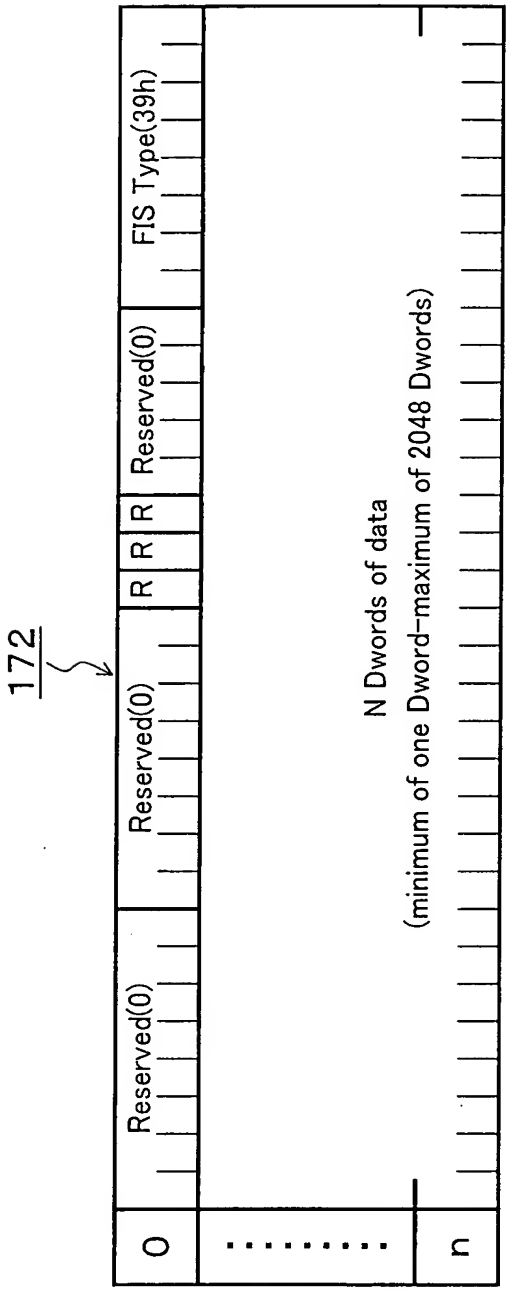

172
0
Reserved(0)
Reserved(0)
R
R
R
Reserved(0)
FIS Type(39h)
N Dwords of data
(minimum of one Dword-maximum of 2048 Dwords)
n

FIG. 13

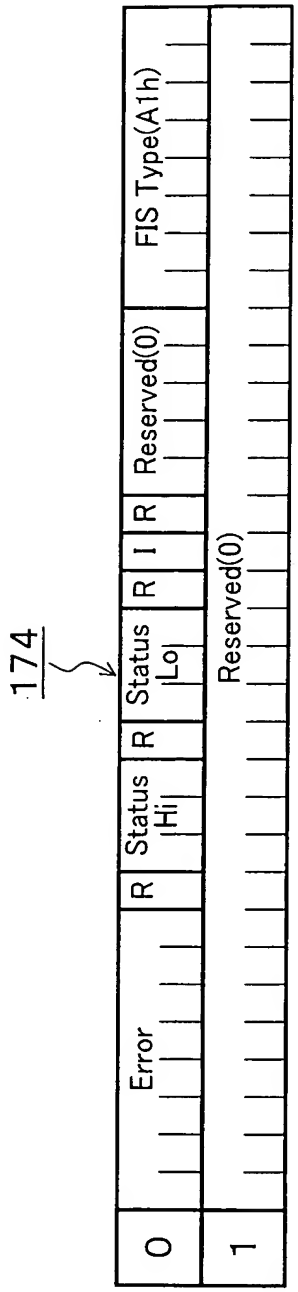

174
FIS Type(A1h)
Reserved(0)
R
I
R
Status Lo
R
Status Hi
R
Error
0
1
Reserved(0)

FIG. 14

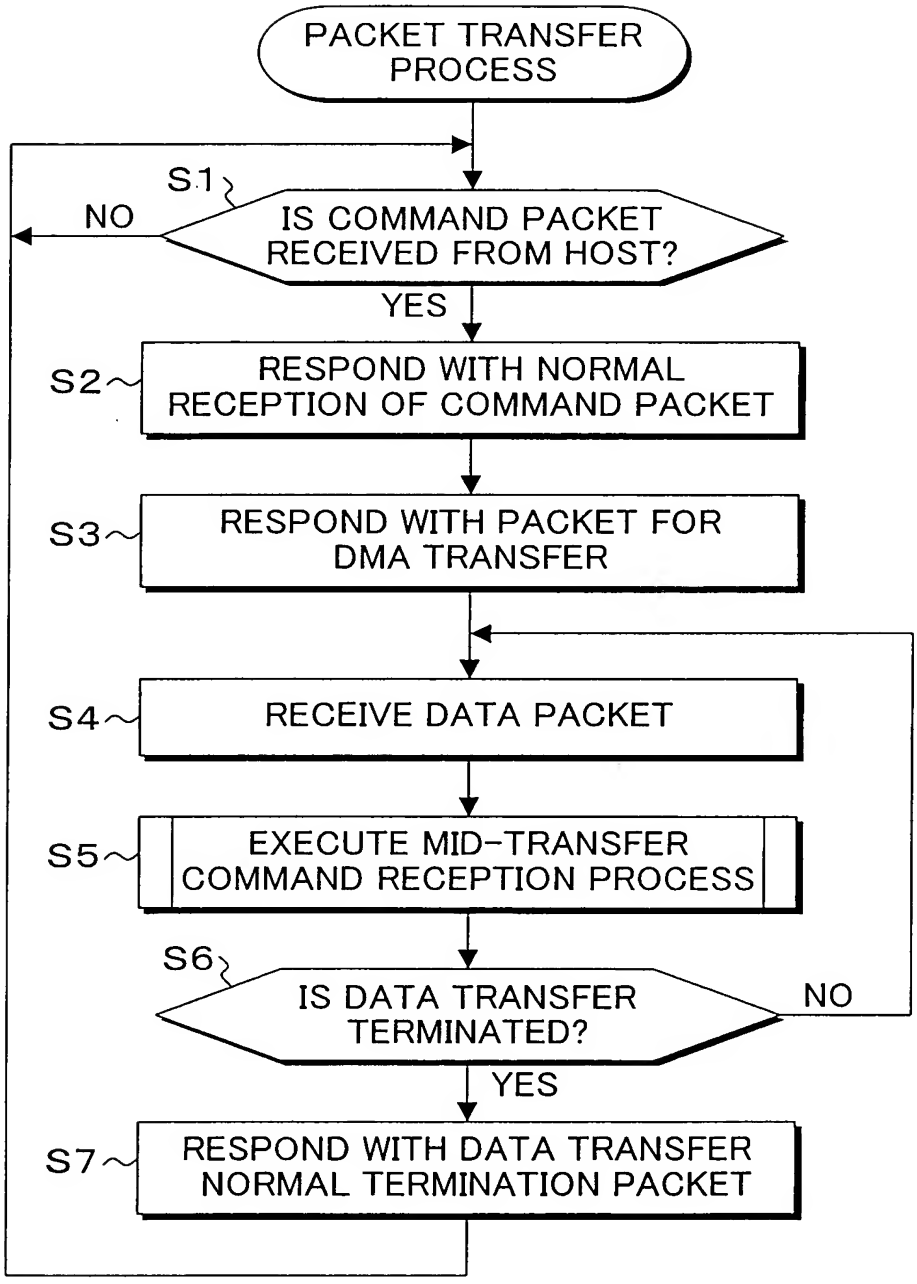

PACKET TRANSFER PROCESS
S1
IS COMMAND PACKET RECEIVED FROM HOST?
NO
YES
S2
RESPOND WITH NORMAL RECEPTION OF COMMAND PACKET
S3
RESPOND WITH PACKET FOR DMA TRANSFER
S4
RECEIVE DATA PACKET
S5
EXECUTE MID-TRANSFER COMMAND RECEPTION PROCESS
S6
IS DATA TRANSFER TERMINATED?
NO
YES
S7
RESPOND WITH DATA TRANSFER NORMAL TERMINATION PACKET

FIG. 15

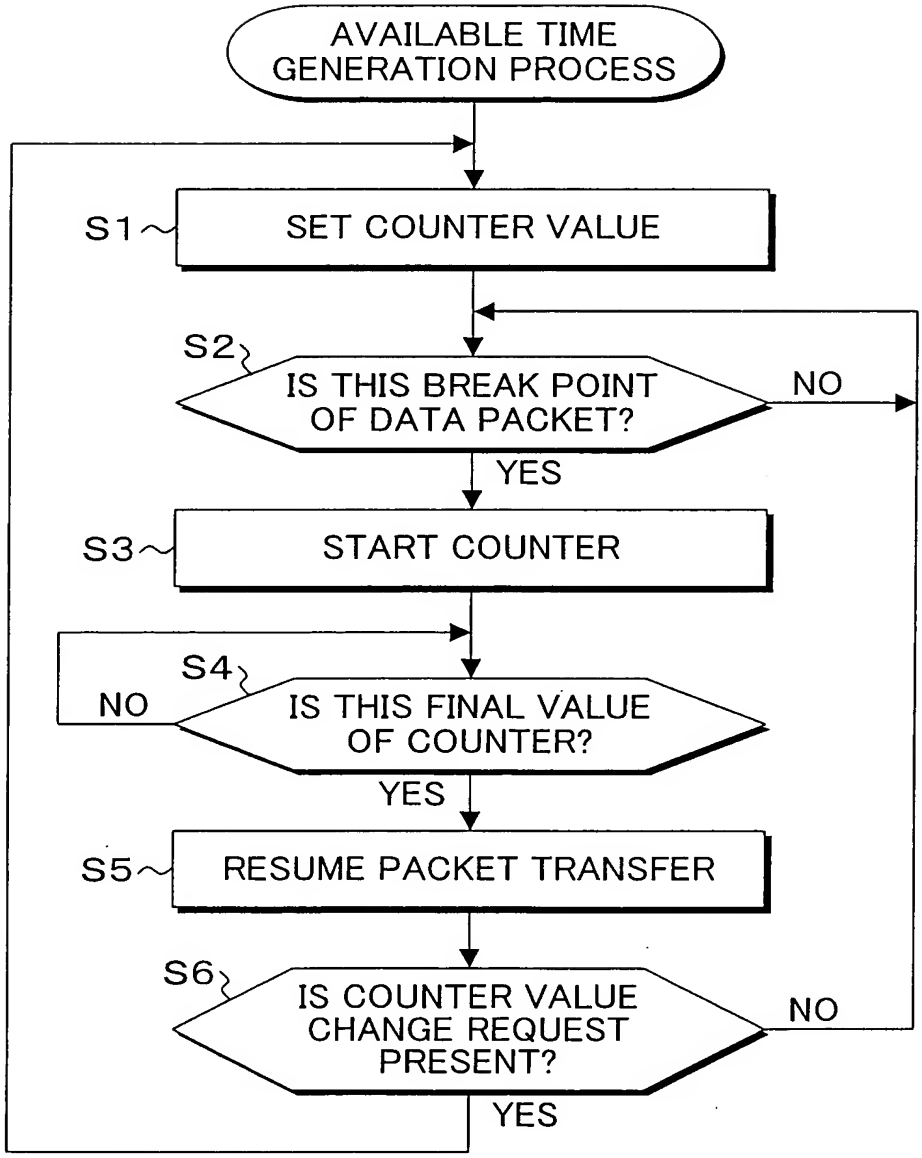

AVAILABLE TIME GENERATION PROCESS
S1
SET COUNTER VALUE
S2
IS THIS BREAK POINT OF DATA PACKET?
NO
YES
S3
START COUNTER
S4
NO
IS THIS FINAL VALUE OF COUNTER?
YES
S5
RESUME PACKET TRANSFER
S6
IS COUNTER VALUE CHANGE REQUEST PRESENT?
NO
YES

FIG. 16A

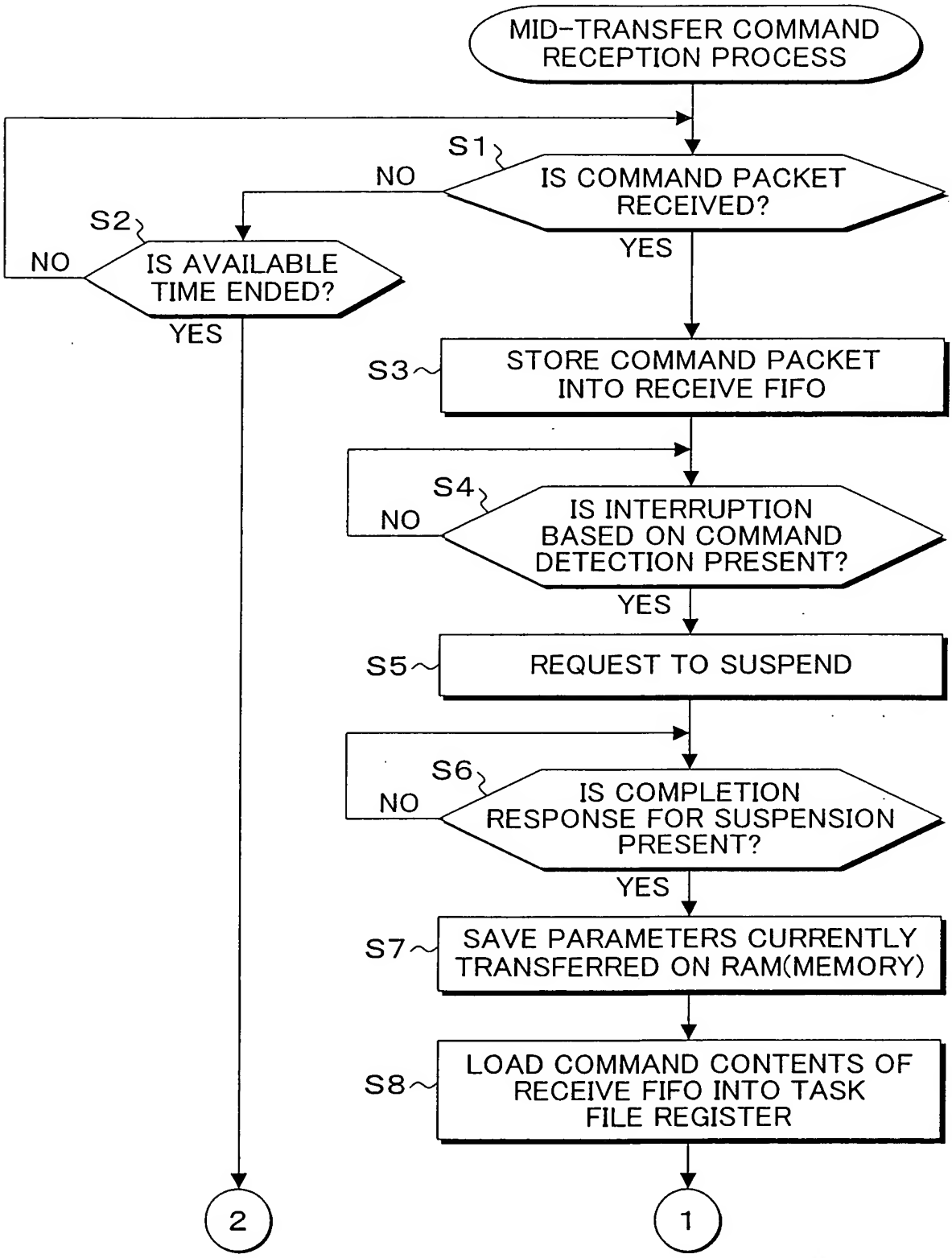

MID-TRANSFER COMMAND RECEPTION PROCESS
S1
IS COMMAND PACKET RECEIVED?
NO
YES
S2
IS AVAILABLE TIME ENDED?
NO
YES
S3
STORE COMMAND PACKET INTO RECEIVE FIFO
S4
IS INTERRUPTION BASED ON COMMAND DETECTION PRESENT?
NO
YES
S5
REQUEST TO SUSPEND
S6
IS COMPLETION RESPONSE FOR SUSPENSION PRESENT?
NO
YES
S7
SAVE PARAMETERS CURRENTLY TRANSFERRED ON RAM(MEMORY)
S8
LOAD COMMAND CONTENTS OF RECEIVE FIFO INTO TASK FILE REGISTER
2
1

FIG. 16B

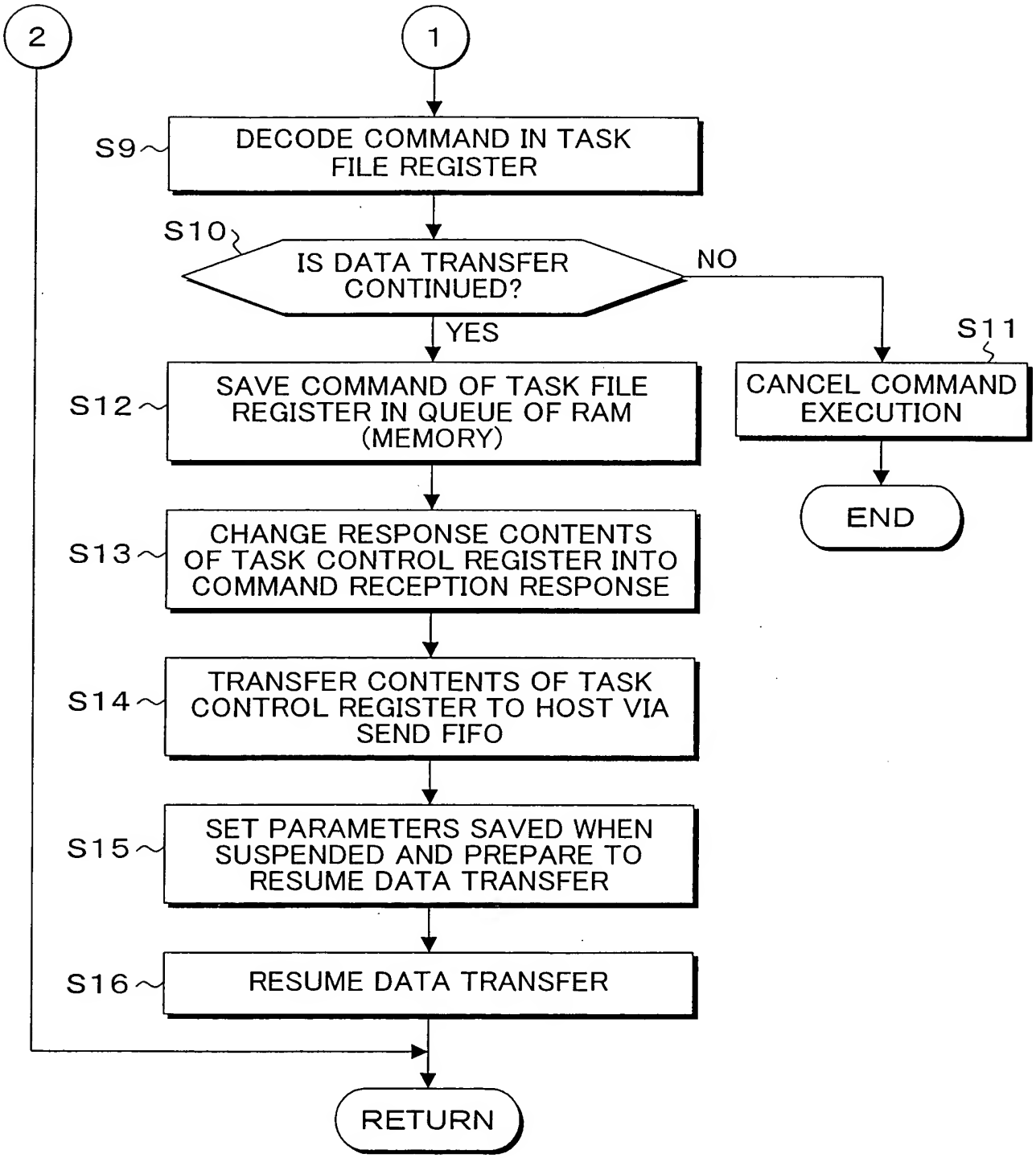

2
1
S9
DECODE COMMAND IN TASK FILE REGISTER
S10
IS DATA TRANSFER CONTINUED?
NO
YES
S11
CANCEL COMMAND EXECUTION
END
S12
SAVE COMMAND OF TASK FILE REGISTER IN QUEUE OF RAM (MEMORY)
S13
CHANGE RESPONSE CONTENTS OF TASK CONTROL REGISTER INTO COMMAND RECEPTION RESPONSE
S14
TRANSFER CONTENTS OF TASK CONTROL REGISTER TO HOST VIA SEND FIFO
S15
SET PARAMETERS SAVED WHEN SUSPENDED AND PREPARE TO RESUME DATA TRANSFER
S16
RESUME DATA TRANSFER
RETURN

FIG. 17

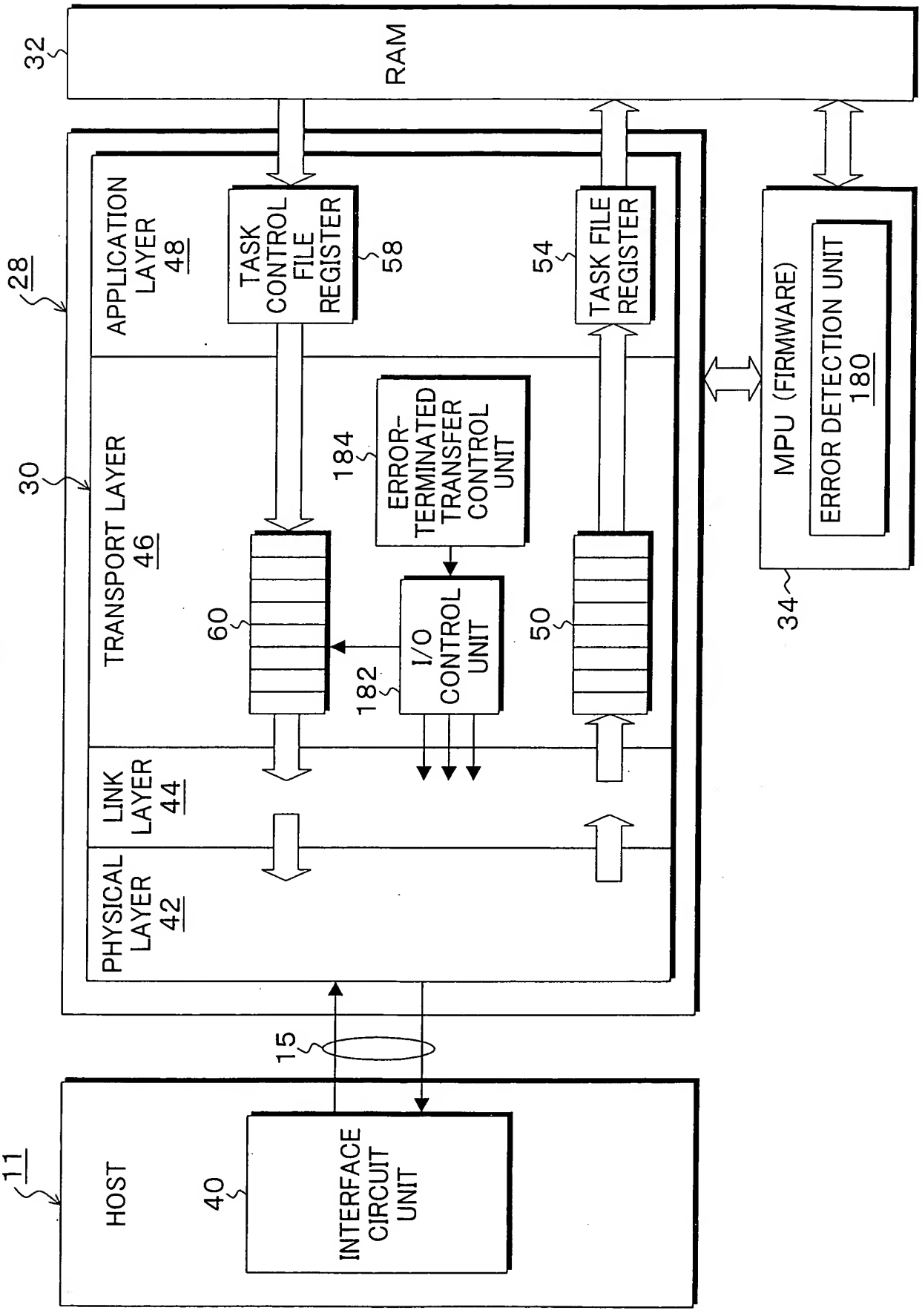

32
RAM
28
APPLICATION LAYER 48
TASK CONTROL FILE REGISTER
58
54
TASK FILE REGISTER
30
TRANSPORT LAYER 46
184
ERROR-TERMINATED TRANSFER CONTROL UNIT
60
182
I/O CONTROL UNIT
50
LINK LAYER 44
PHYSICAL LAYER 42
MPU (FIRMWARE)
ERROR DETECTION UNIT 180
34
15
11
HOST
40
INTERFACE CIRCUIT UNIT

FIG. 18A

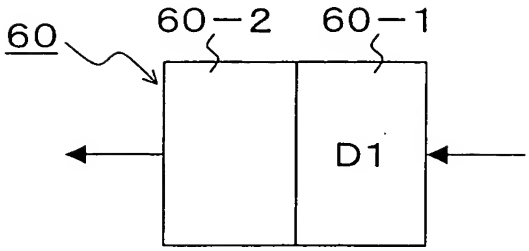


FIG. 18B

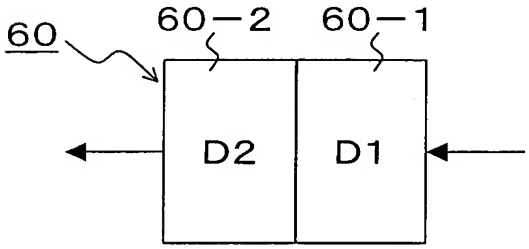


FIG. 18C

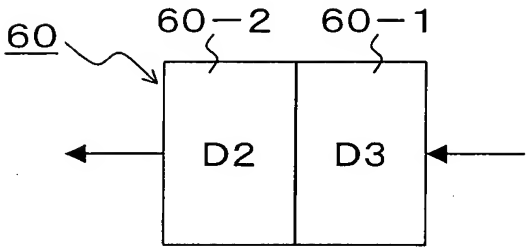
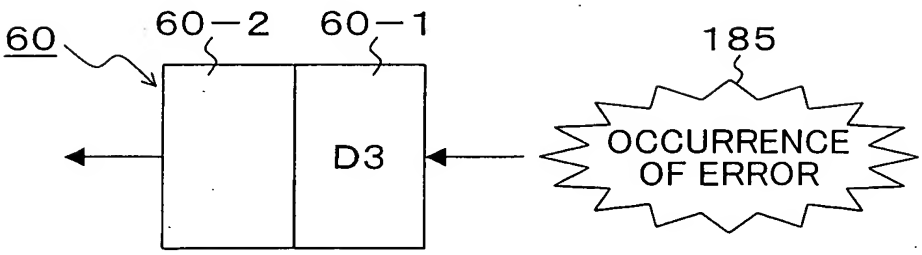


FIG. 18D



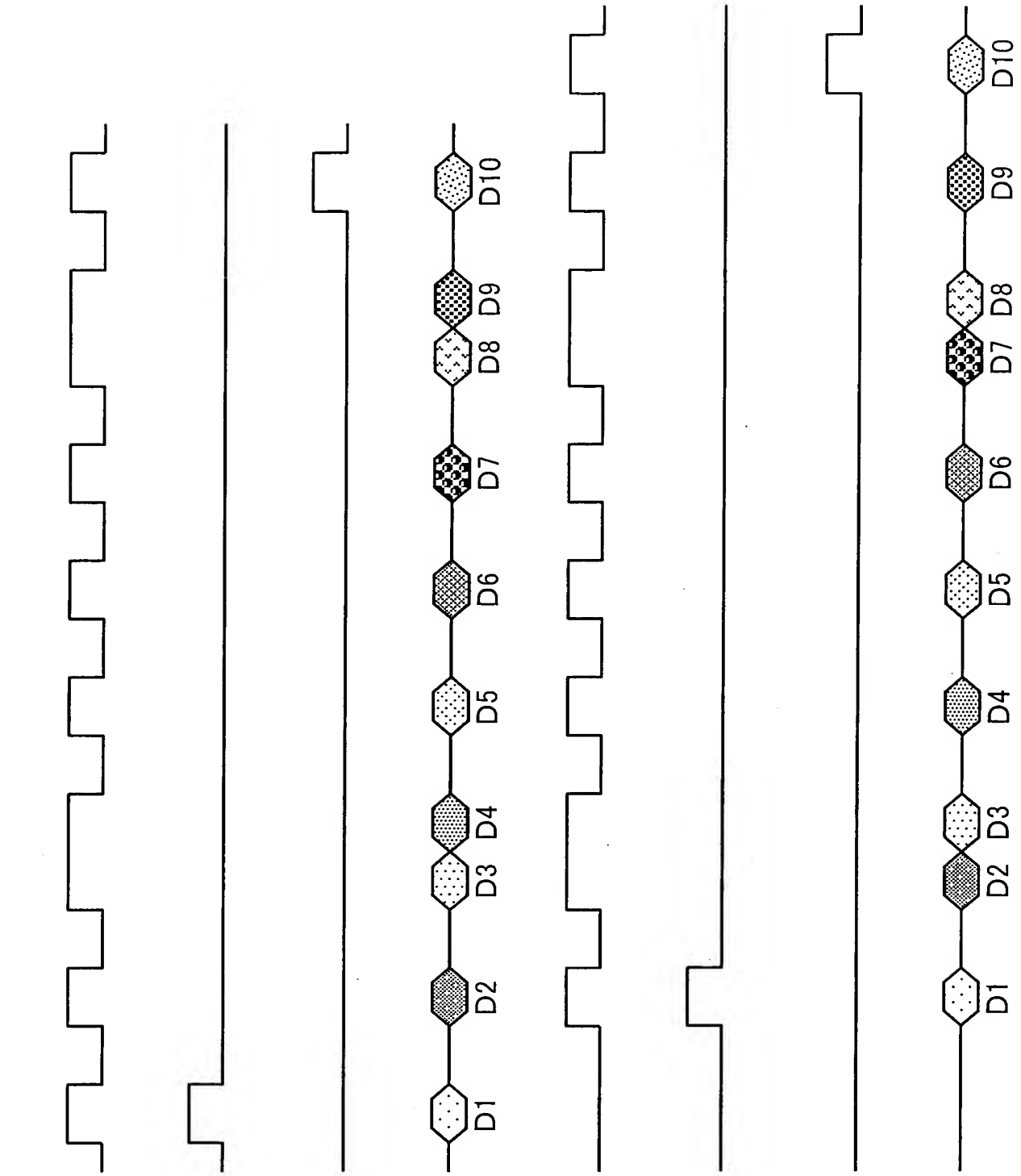


FIG. 19A
INPUT VALID SIGNAL

FIG. 19B
INPUT HEAD SIGNAL

FIG. 19C
INPUT TAIL SIGNAL

FIG. 19D
INPUT DATA

FIG. 19E
OUTPUT VALID SIGNAL

FIG. 19F
OUTPUT HEAD SIGNAL

FIG. 19G
OUTPUT TAIL SIGNAL

FIG. 19H
OUTPUT DATA

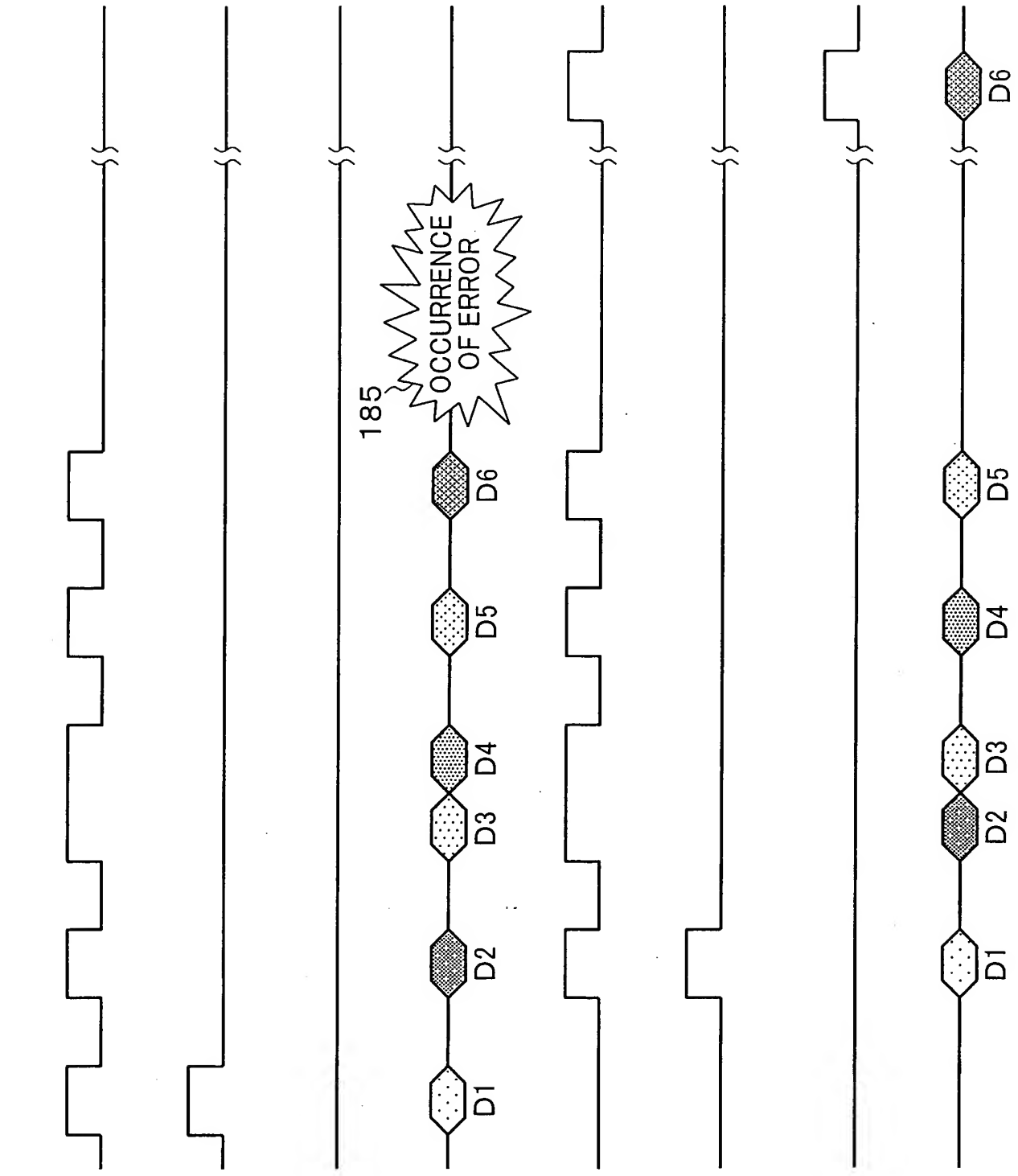


FIG. 20A
INPUT VALID SIGNAL

FIG. 20B
INPUT HEAD SIGNAL

FIG. 20C
INPUT TAIL SIGNAL

FIG. 20D
INPUT DATA

FIG. 20E
OUTPUT VALID SIGNAL

FIG. 20F
OUTPUT HEAD SIGNAL

FIG. 20G
OUTPUT TAIL SIGNAL

FIG. 20H
OUTPUT DATA

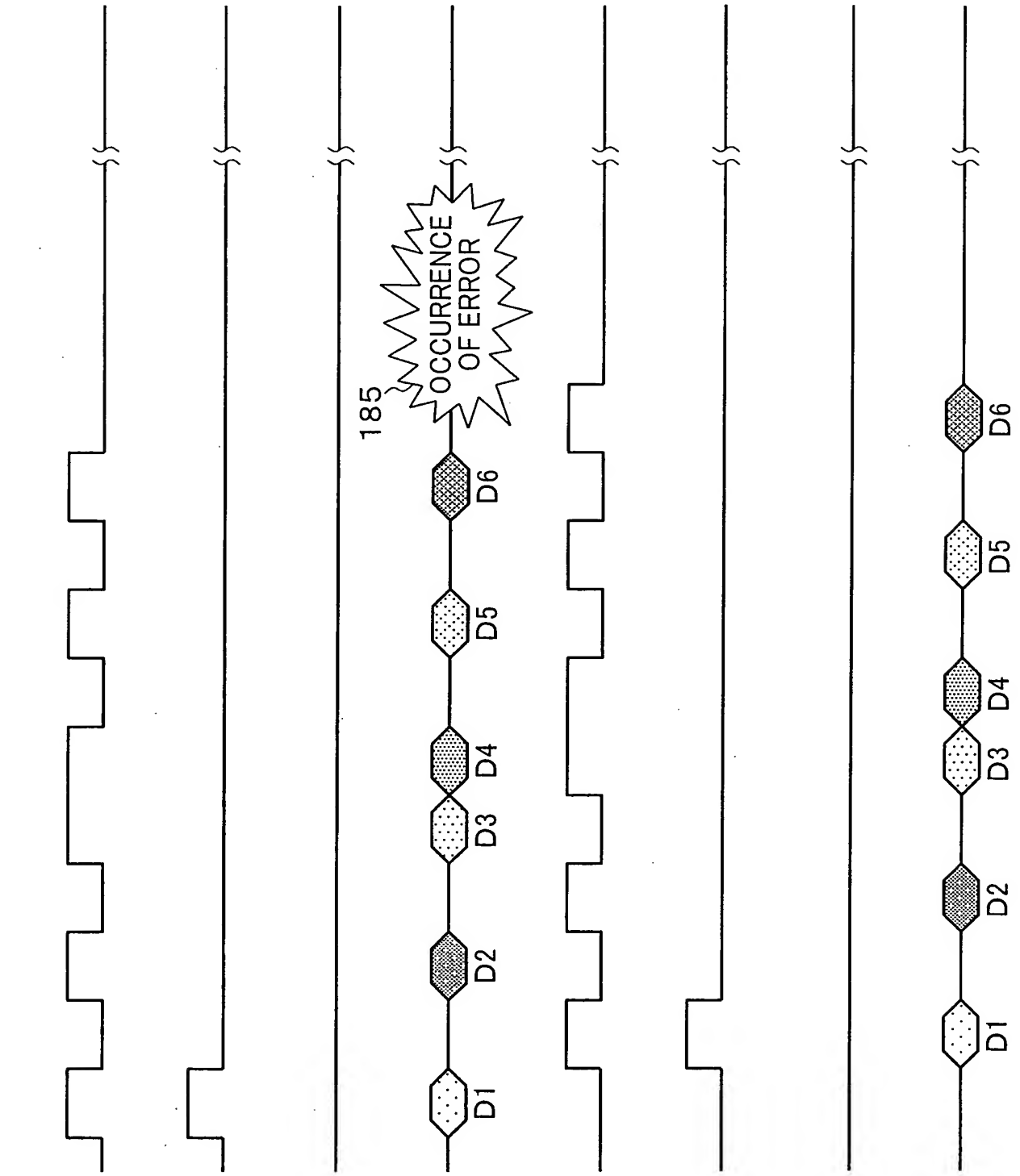


FIG. 21A INPUT VALID SIGNAL

FIG. 21B INPUT HEAD SIGNAL

FIG. 21C INPUT TAIL SIGNAL

FIG. 21D INPUT DATA

FIG. 21E OUTPUT VALID SIGNAL

FIG. 21F OUTPUT HEAD SIGNAL

FIG. 21G OUTPUT TAIL SIGNAL

FIG. 21H OUTPUT DATA

FIG. 22

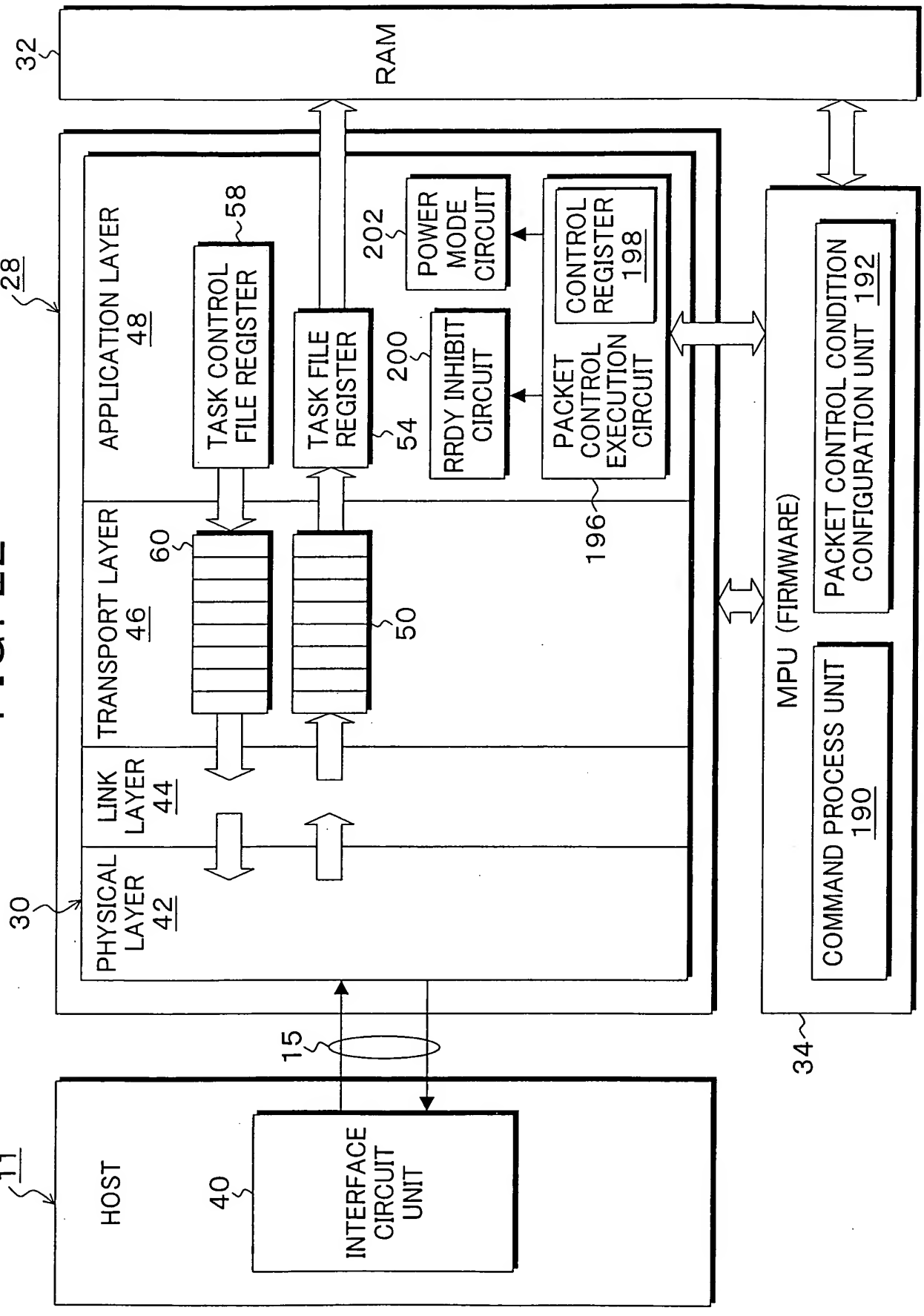

32
RAM
28
APPLICATION LAYER
48
58
TASK CONTROL FILE REGISTER
202
POWER MODE CIRCUIT
CONTROL REGISTER
198
TASK FILE REGISTER
54
200
RRDY INHIBIT CIRCUIT
PACKET CONTROL EXECUTION CIRCUIT
196
TRANSPORT LAYER
46
60
50
LINK LAYER
44
PHYSICAL LAYER
42
30
MPU (FIRMWARE)
PACKET CONTROL CONDITION CONFIGURATION UNIT
192
COMMAND PROCESS UNIT
190
34
15
11
HOST
40
INTERFACE CIRCUIT UNIT

FIG. 23

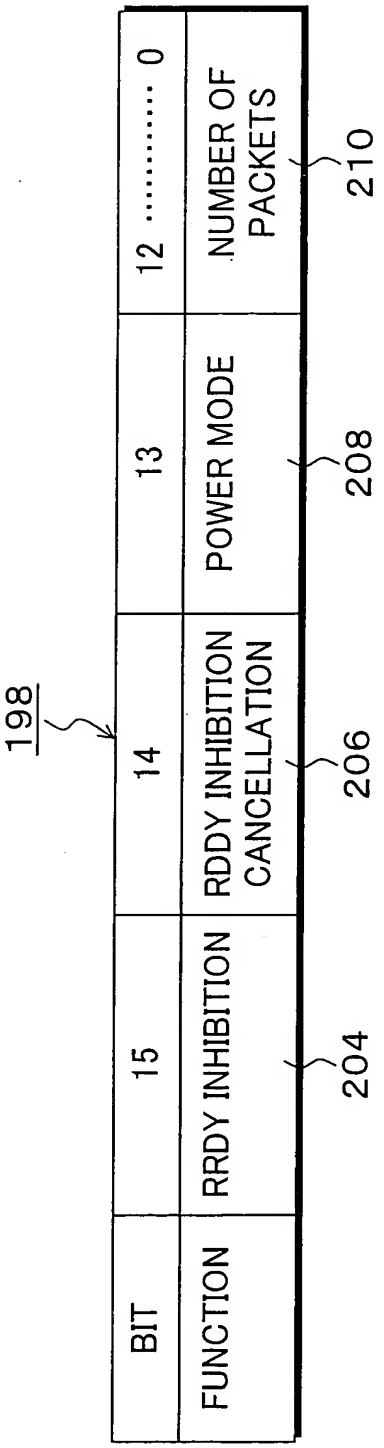

198
BIT
FUNCTION
15
RRDY INHIBITION
204
14
RDDY INHIBITION CANCELLATION
206
13
POWER MODE
208
12 0
NUMBER OF PACKETS
210

FIG. 24

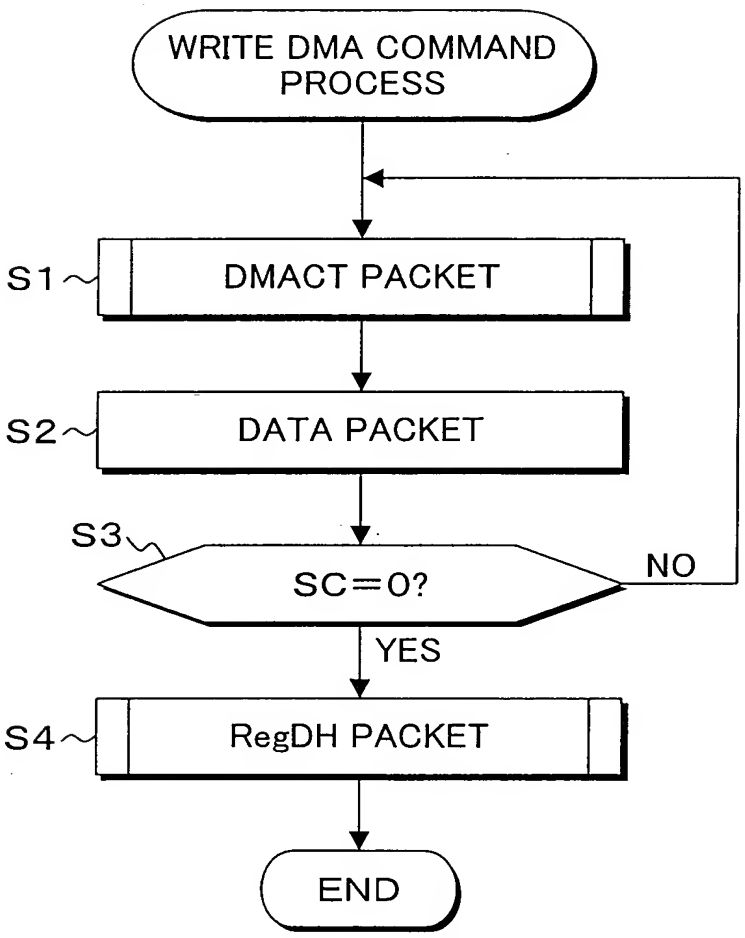

WRITE DMA COMMAND PROCESS
S1
DMACT PACKET
S2
DATA PACKET
S3
SC=0?
NO
YES
S4
RegDH PACKET
END

FIG. 25

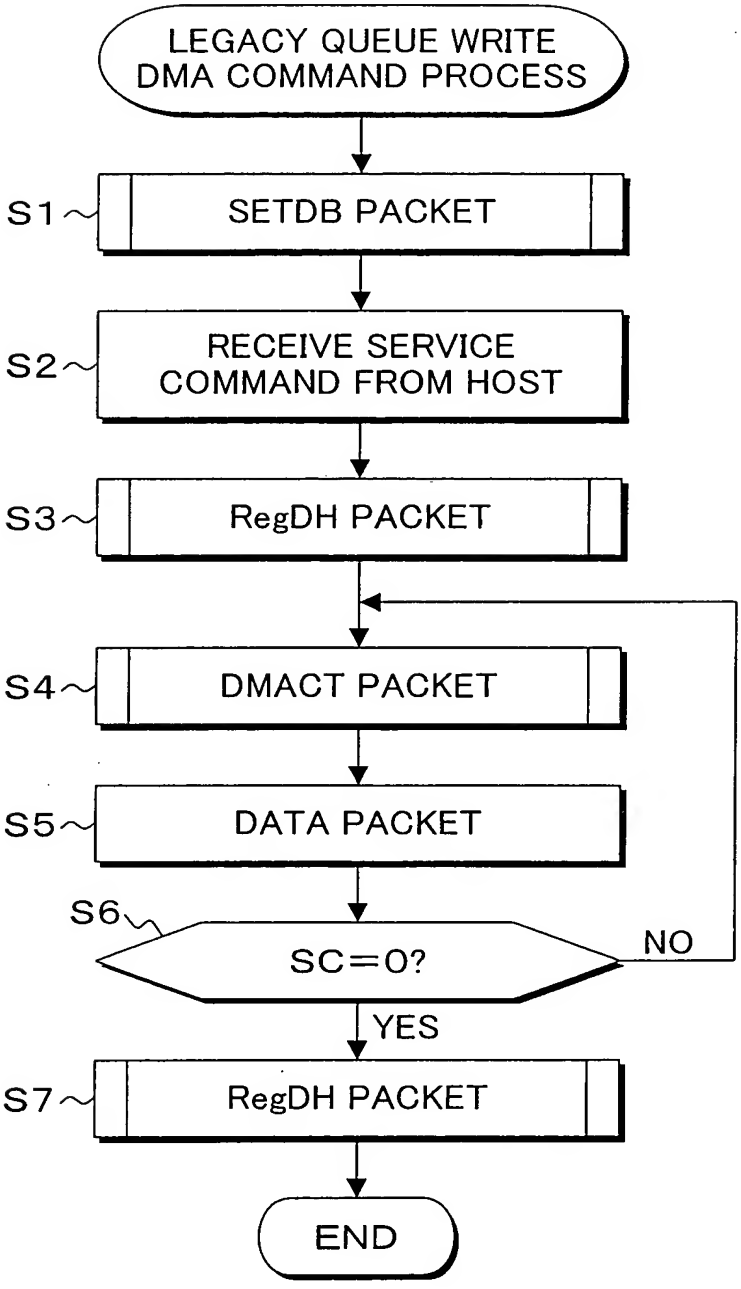

LEGACY QUEUE WRITE DMA COMMAND PROCESS
S1
SETDB PACKET
S2
RECEIVE SERVICE COMMAND FROM HOST
S3
RegDH PACKET
S4
DMACT PACKET
S5
DATA PACKET
S6
SC=0?
NO
YES
S7
RegDH PACKET
END

FIG. 26

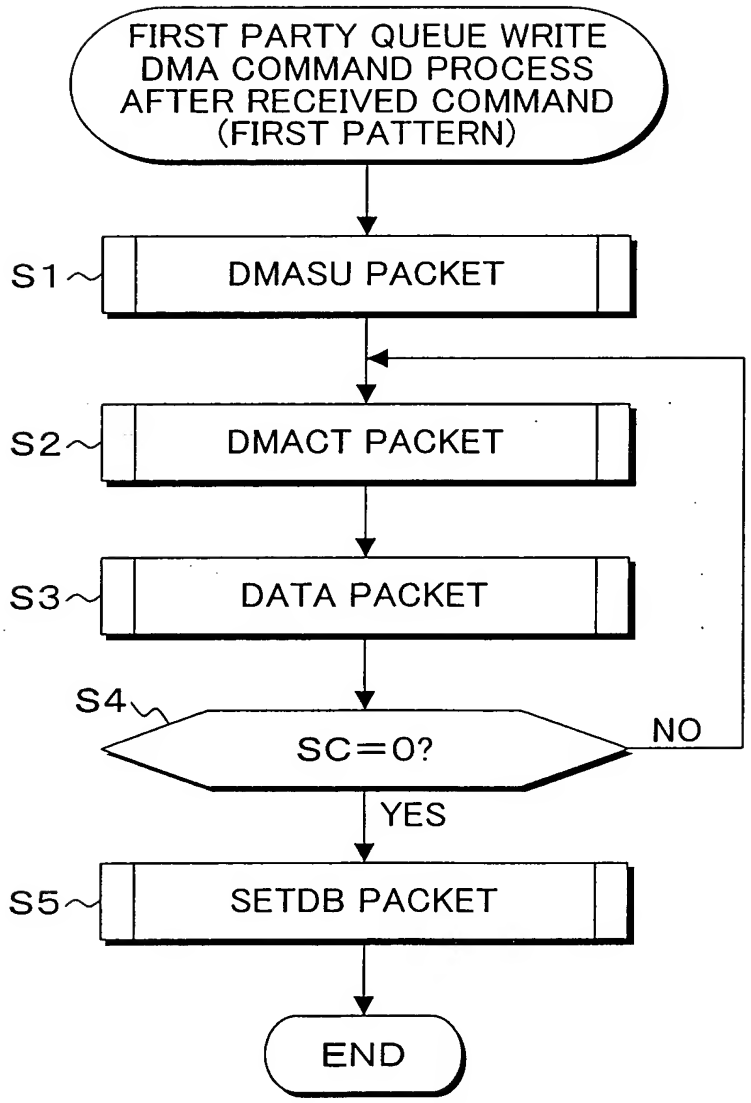

FIRST PARTY QUEUE WRITE DMA COMMAND PROCESS AFTER RECEIVED COMMAND (FIRST PATTERN)
S1
DMASU PACKET
S2
DMACT PACKET
S3
DATA PACKET
S4
SC=0?
NO
YES
S5
SETDB PACKET
END

FIG. 27

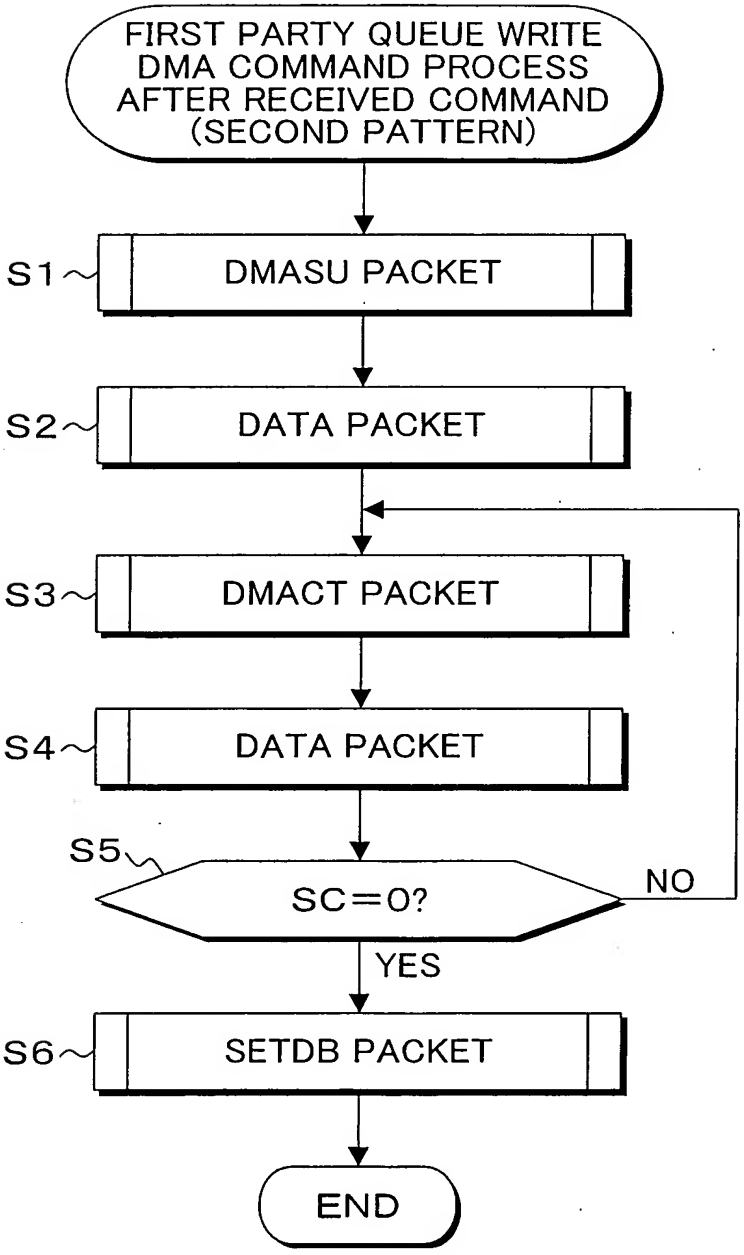

FIRST PARTY QUEUE WRITE DMA COMMAND PROCESS AFTER RECEIVED COMMAND (SECOND PATTERN)
S1
DMASU PACKET
S2
DATA PACKET
S3
DMACT PACKET
S4
DATA PACKET
S5
SC=0?
NO
YES
S6
SETDB PACKET
END

FIG. 28A

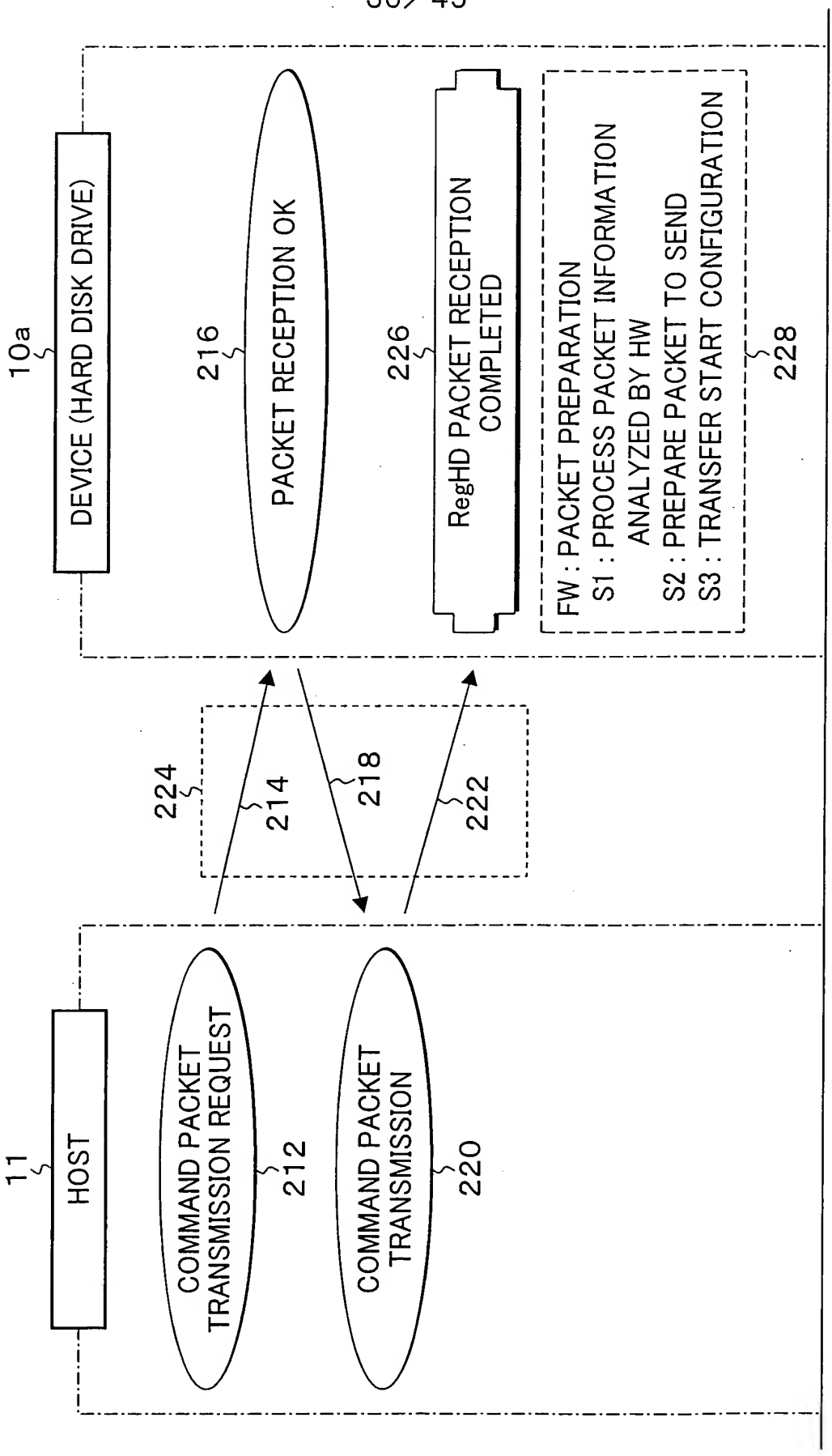

10a
DEVICE (HARD DISK DRIVE)
216
PACKET RECEPTION OK
226
RegHD PACKET RECEPTION COMPLETED
FW : PACKET PREPARATION
S1 : PROCESS PACKET INFORMATION ANALYZED BY HW
S2 : PREPARE PACKET TO SEND
S3 : TRANSFER START CONFIGURATION
228
224
214
218
222
11
HOST
COMMAND PACKET TRANSMISSION REQUEST
212
COMMAND PACKET TRANSMISSION
220

FIG. 28B

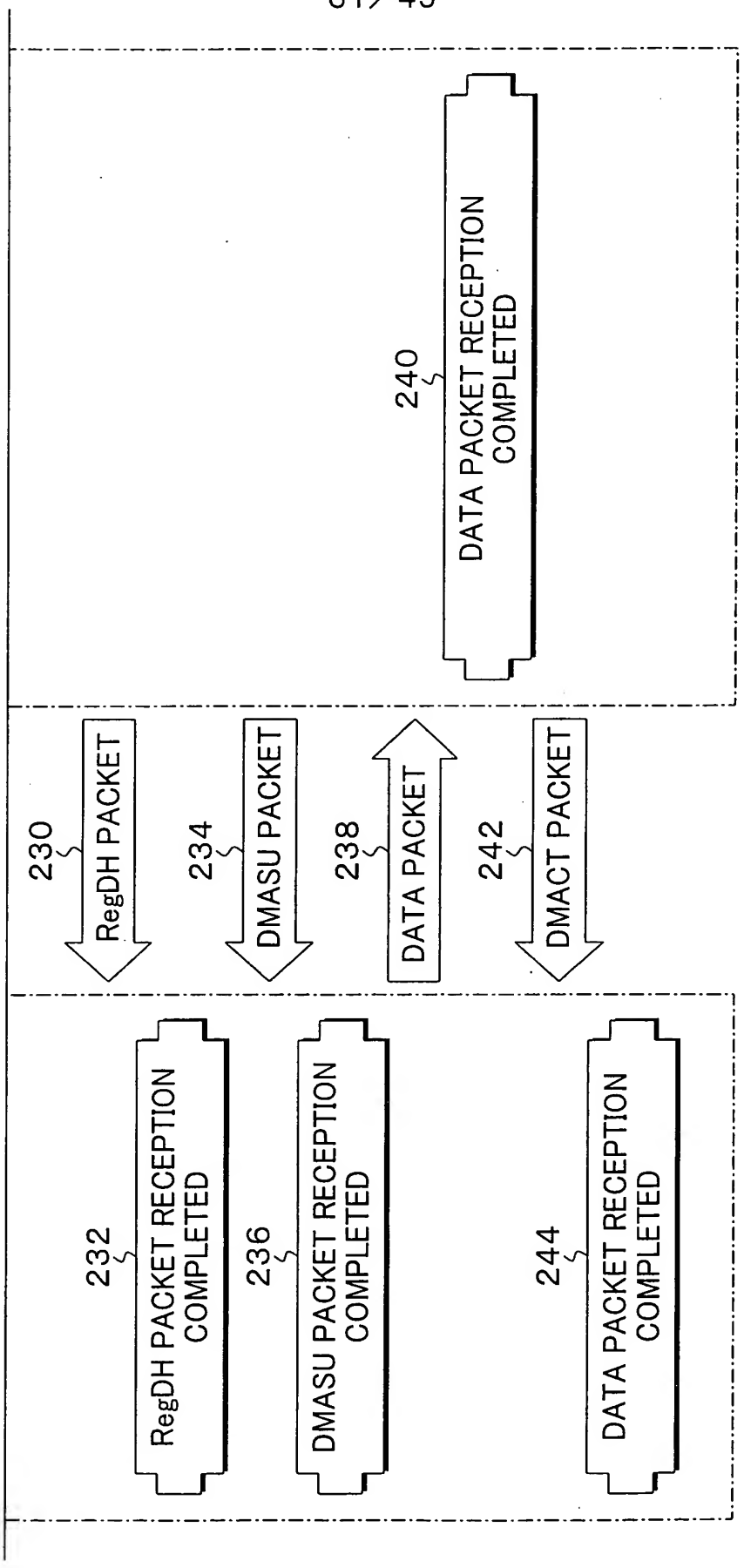

240
DATA PACKET RECEPTION COMPLETED
230
RegDH PACKET
234
DMASU PACKET
238
DATA PACKET
242
DMACT PACKET
232
RegDH PACKET RECEPTION COMPLETED
236
DMASU PACKET RECEPTION COMPLETED
244
DATA PACKET RECEPTION COMPLETED

FIG. 29A

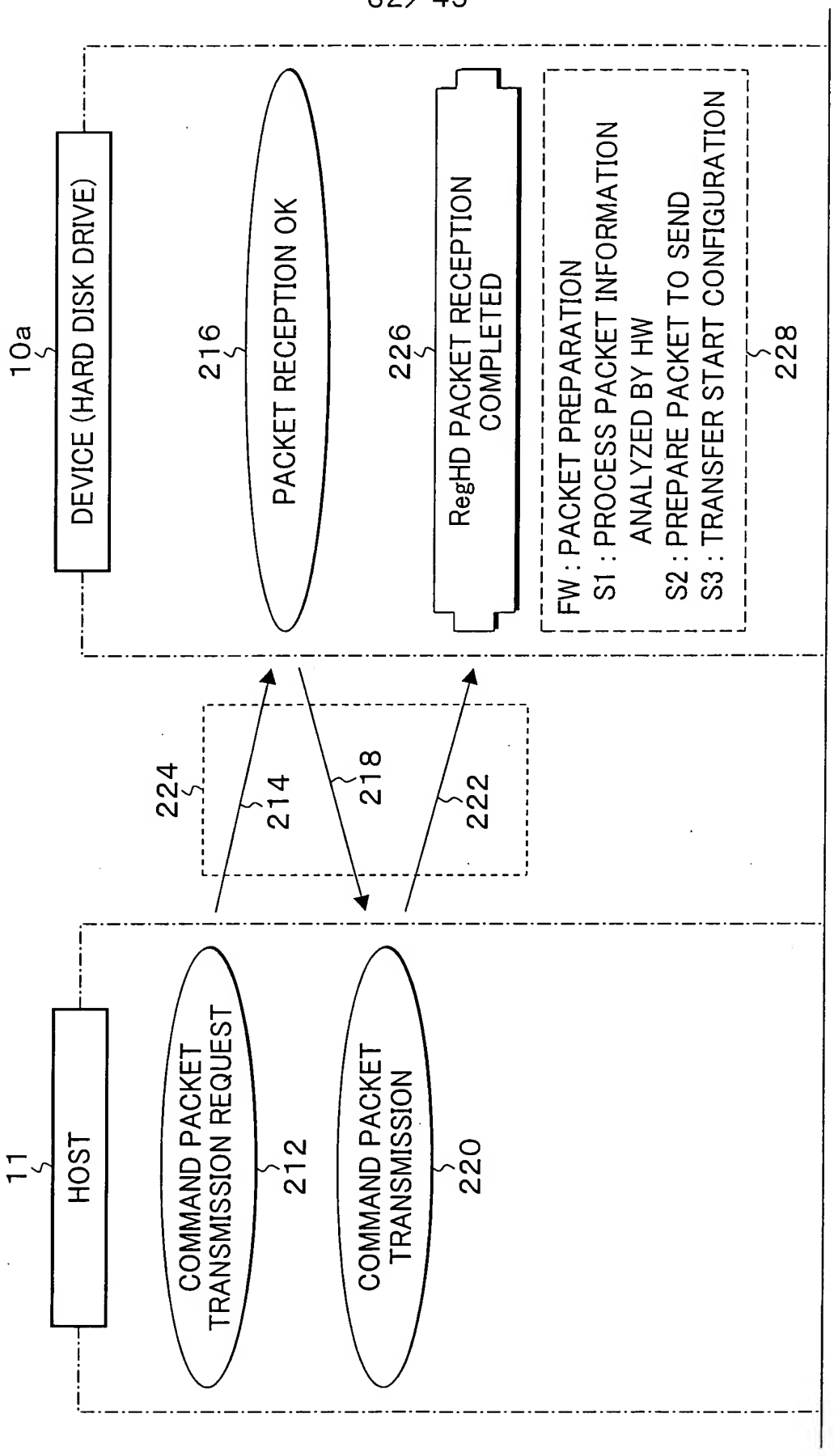

10a
DEVICE (HARD DISK DRIVE)
216
PACKET RECEPTION OK
226
RegHD PACKET RECEPTION COMPLETED
FW : PACKET PREPARATION
S1 : PROCESS PACKET INFORMATION ANALYZED BY HW
S2 : PREPARE PACKET TO SEND
S3 : TRANSFER START CONFIGURATION
228
224
214
218
222
11
HOST
COMMAND PACKET TRANSMISSION REQUEST
212
COMMAND PACKET TRANSMISSION
220

FIG. 29B

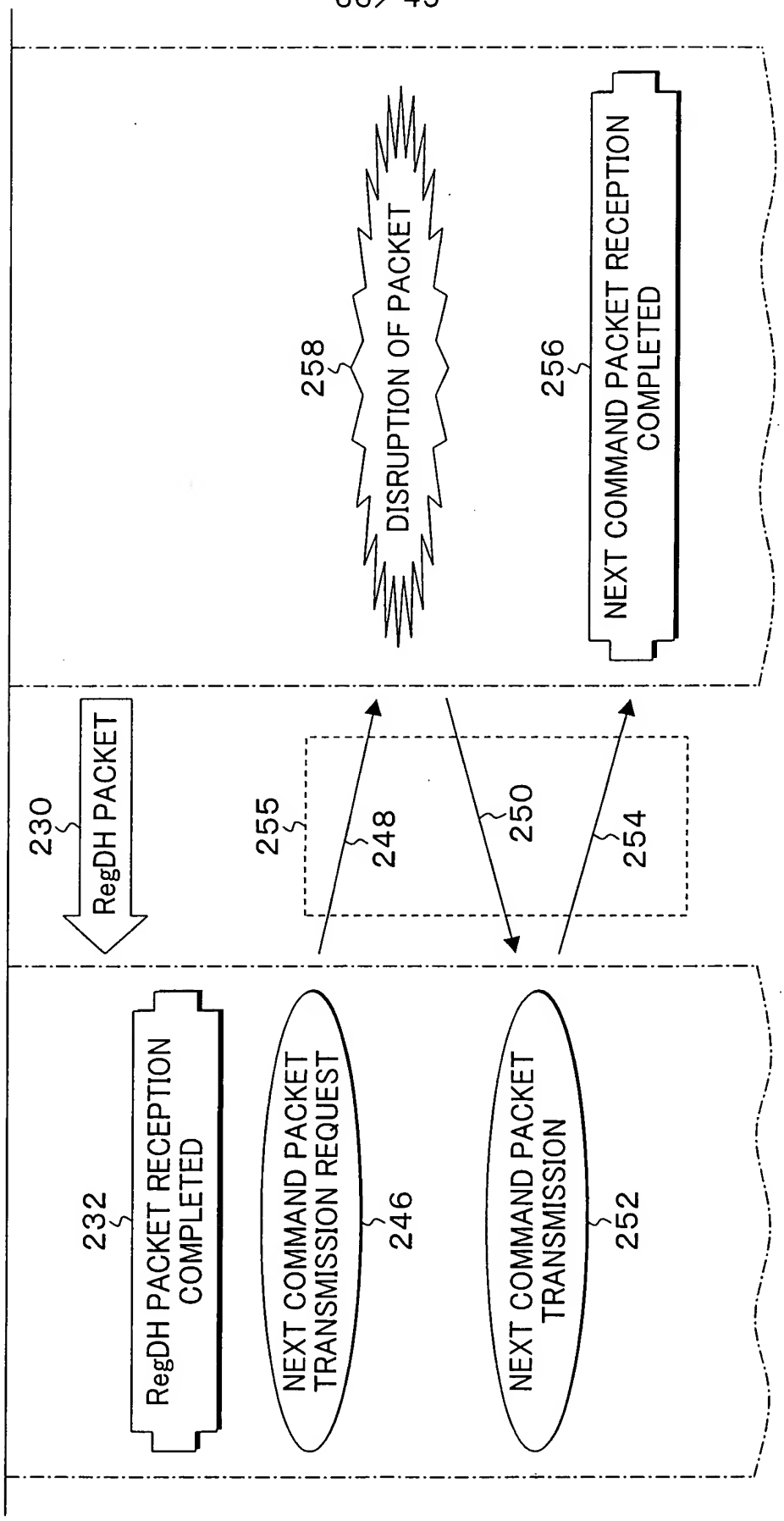

230
RegDH PACKET
255
248
250
254
258
DISRUPTION OF PACKET
256
NEXT COMMAND PACKET RECEPTION COMPLETED
232
RegDH PACKET RECEPTION COMPLETED
NEXT COMMAND PACKET TRANSMISSION REQUEST
246
NEXT COMMAND PACKET TRANSMISSION
252

FIG. 30A

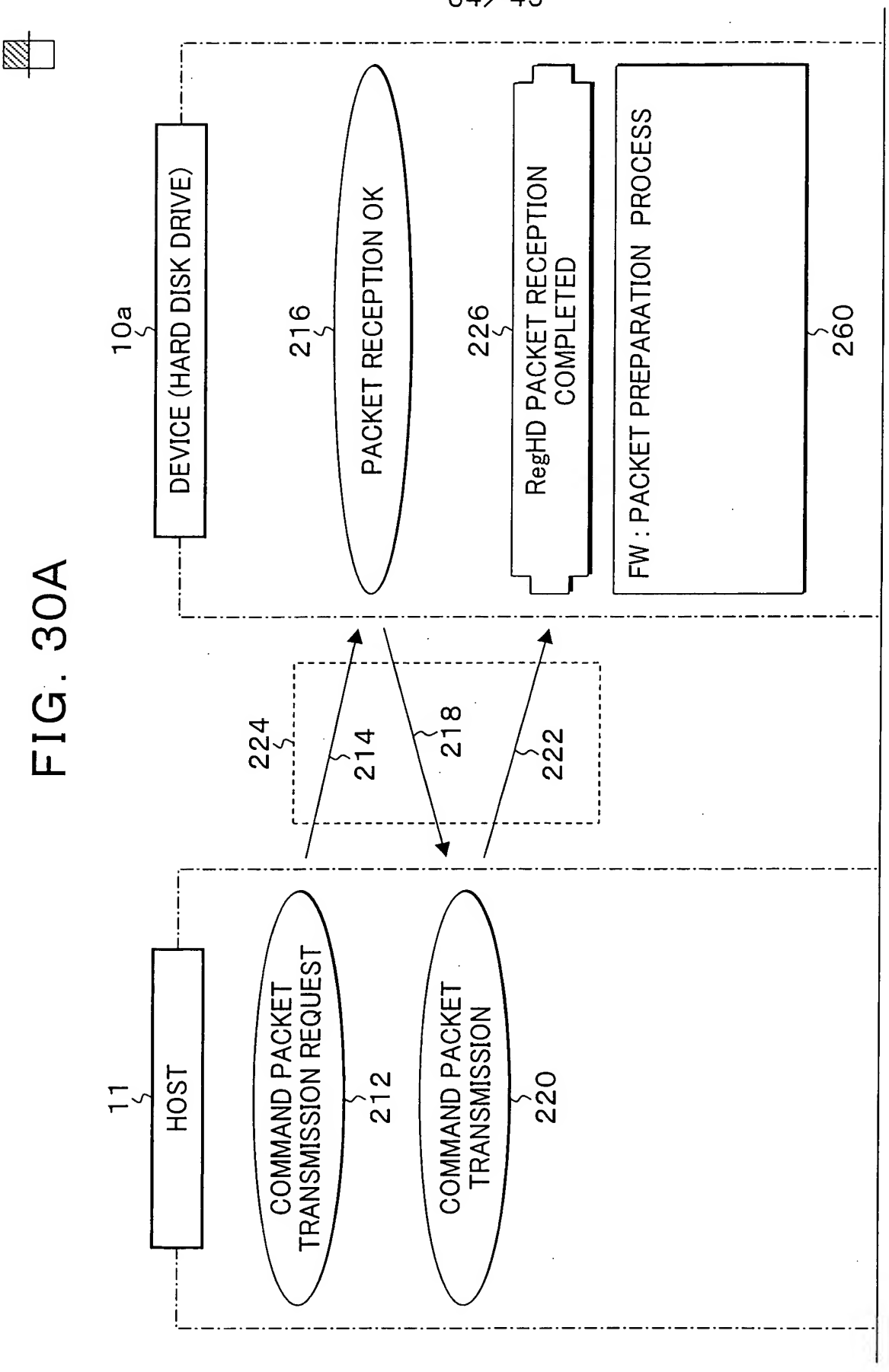

10a
DEVICE (HARD DISK DRIVE)
216
PACKET RECEPTION OK
226
RegHD PACKET RECEPTION COMPLETED
260
FW : PACKET PREPARATION PROCESS
224
214
218
222
11
HOST
COMMAND PACKET TRANSMISSION REQUEST
212
COMMAND PACKET TRANSMISSION
220

FIG. 30B

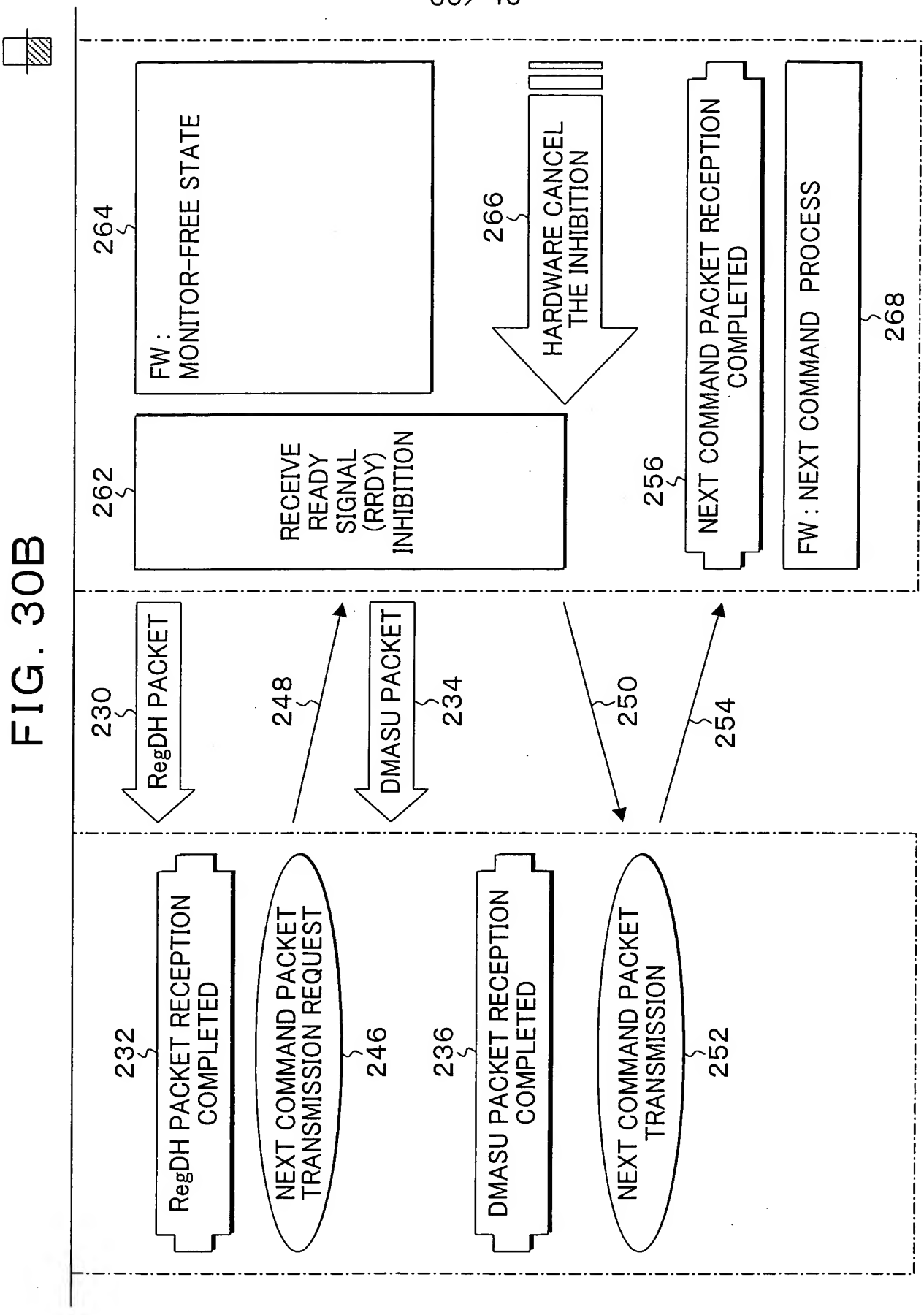

264
FW : MONITOR-FREE STATE
266
HARDWARE CANCEL THE INHIBITION
262
RECEIVE READY SIGNAL (RRDY) INHIBITION
256
NEXT COMMAND PACKET RECEPTION COMPLETED
FW : NEXT COMMAND PROCESS
268
230
RegDH PACKET
248
DMASU PACKET
234
250
254
232
RegDH PACKET RECEPTION COMPLETED
NEXT COMMAND PACKET TRANSMISSION REQUEST
246
236
DMASU PACKET RECEPTION COMPLETED
NEXT COMMAND PACKET TRANSMISSION
252

FIG. 31

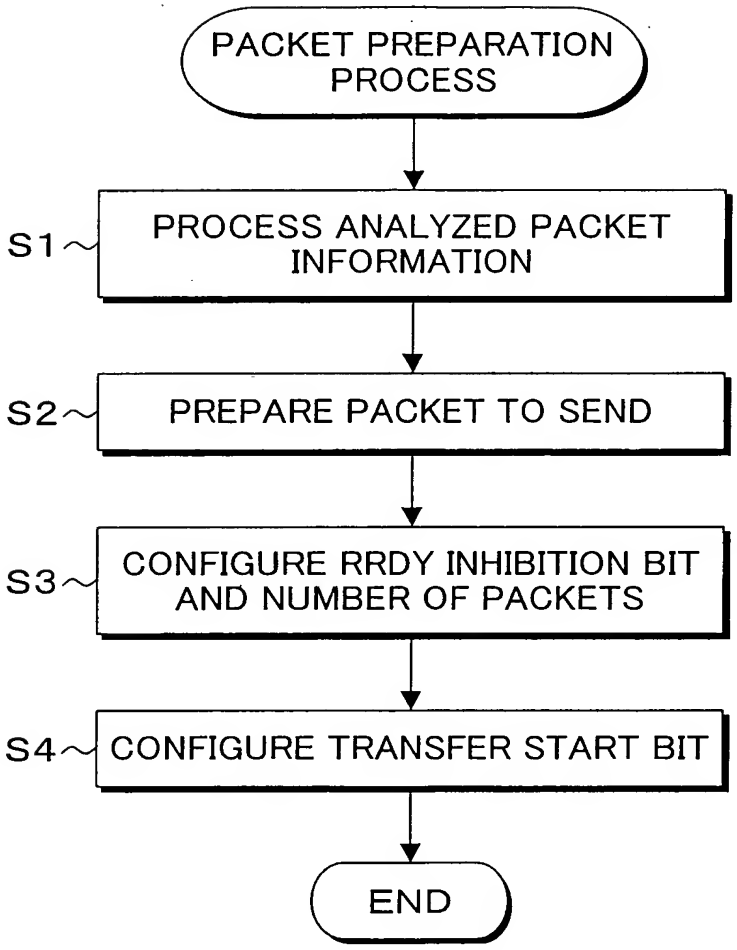

PACKET PREPARATION PROCESS
S1
PROCESS ANALYZED PACKET INFORMATION
S2
PREPARE PACKET TO SEND
S3
CONFIGURE RRDY INHIBITION BIT AND NUMBER OF PACKETS
S4
CONFIGURE TRANSFER START BIT
END

FIG. 32

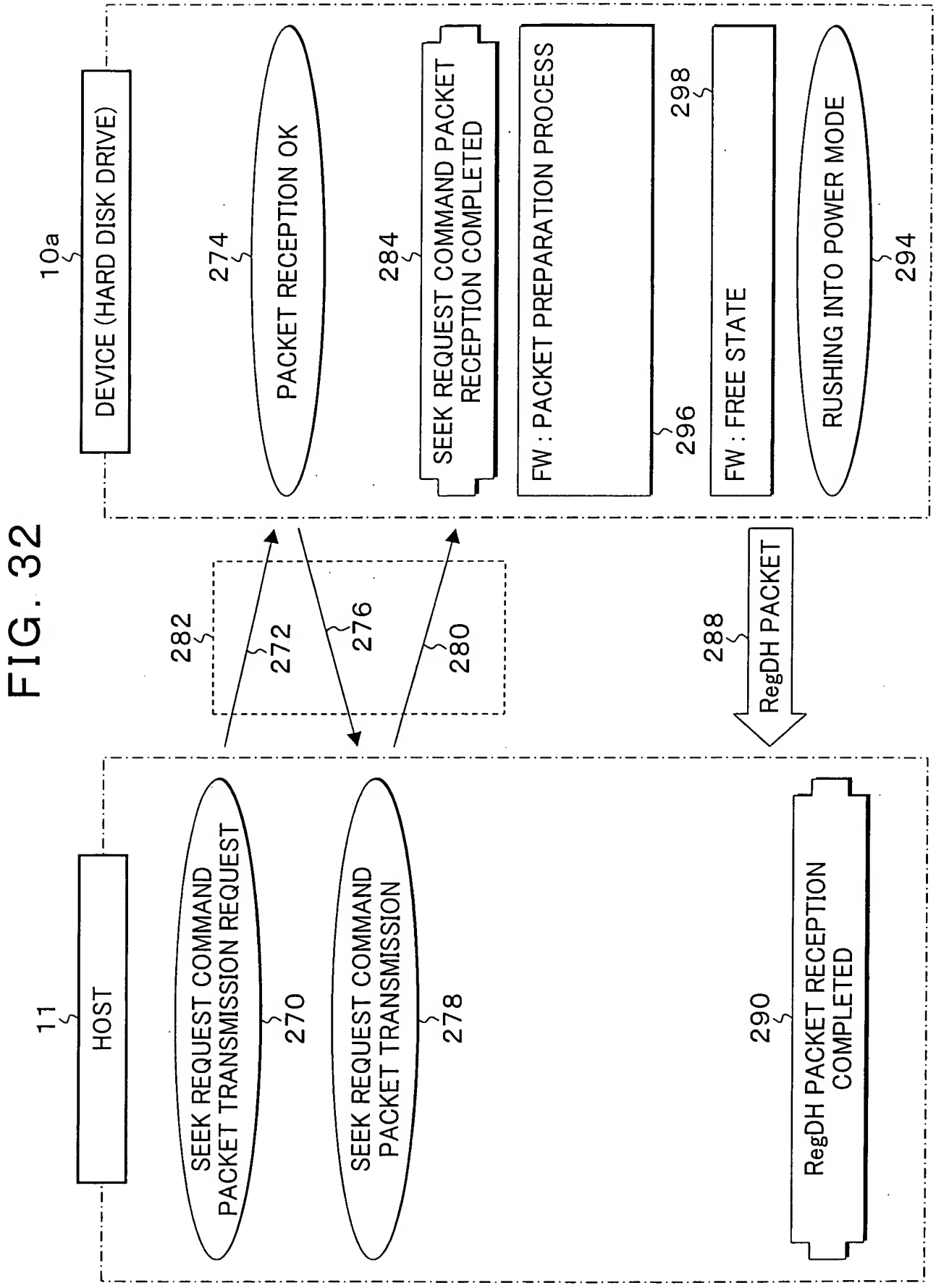

10a
DEVICE (HARD DISK DRIVE)
274
PACKET RECEPTION OK
284
SEEK REQUEST COMMAND PACKET RECEPTION COMPLETED
FW : PACKET PREPARATION PROCESS
296
298
FW : FREE STATE
RUSHING INTO POWER MODE
294
282
272
276
280
288
RegDH PACKET
11
HOST
SEEK REQUEST COMMAND PACKET TRANSMISSION REQUEST
270
SEEK REQUEST COMMAND PACKET TRANSMISSION
278
290
RegDH PACKET RECEPTION COMPLETED

FIG. 33

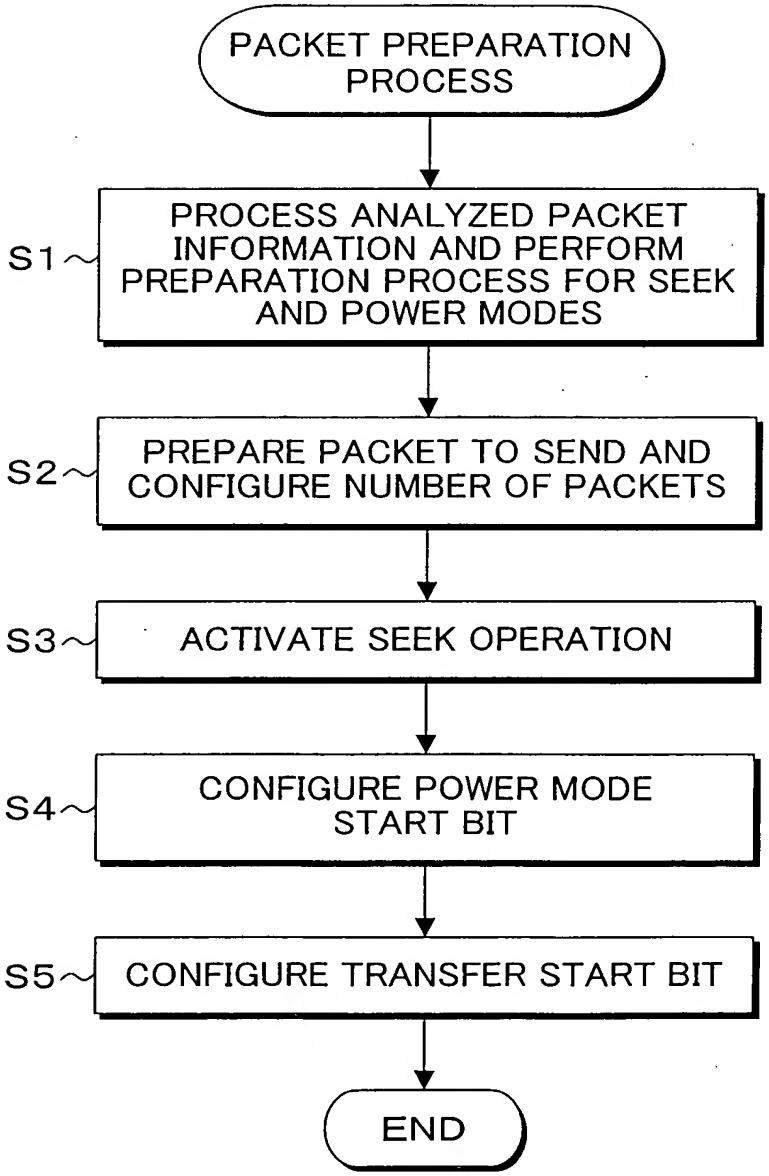

PACKET PREPARATION PROCESS
S1
PROCESS ANALYZED PACKET INFORMATION AND PERFORM PREPARATION PROCESS FOR SEEK AND POWER MODES
S2
PREPARE PACKET TO SEND AND CONFIGURE NUMBER OF PACKETS
S3
ACTIVATE SEEK OPERATION
S4
CONFIGURE POWER MODE START BIT
S5
CONFIGURE TRANSFER START BIT
END

FIG. 34

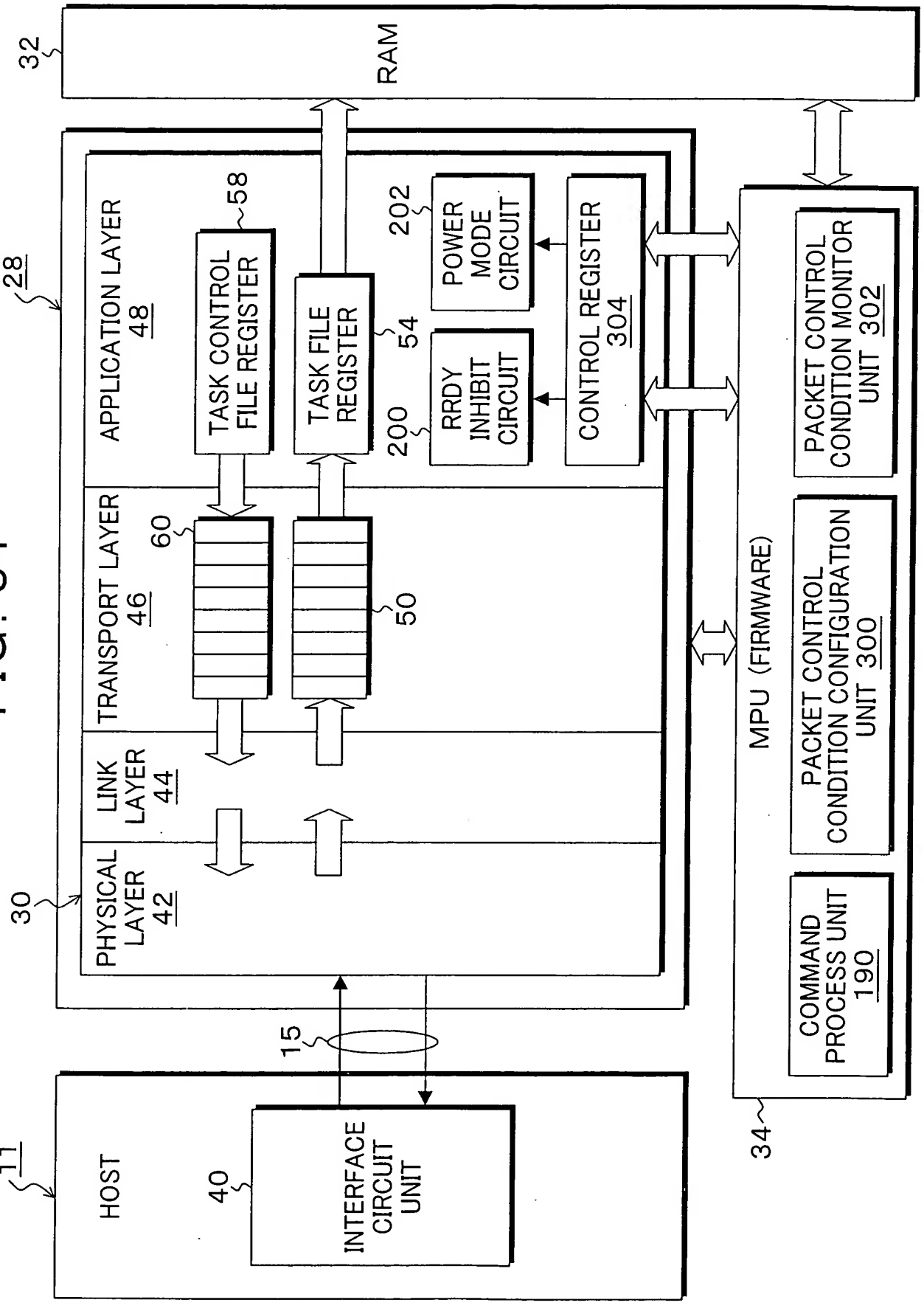

32
RAM
28
APPLICATION LAYER 48
TRANSPORT LAYER 46
LINK LAYER 44
PHYSICAL LAYER 42
30
58
TASK CONTROL FILE REGISTER
54
TASK FILE REGISTER
60
50
202
POWER MODE CIRCUIT
200
RRDY INHIBIT CIRCUIT
CONTROL REGISTER 304
PACKET CONTROL CONDITION MONITOR UNIT 302
PACKET CONTROL CONDITION CONFIGURATION UNIT 300
COMMAND PROCESS UNIT 190
MPU (FIRMWARE)
34
15
11
HOST
40
INTERFACE CIRCUIT UNIT

FIG. 35

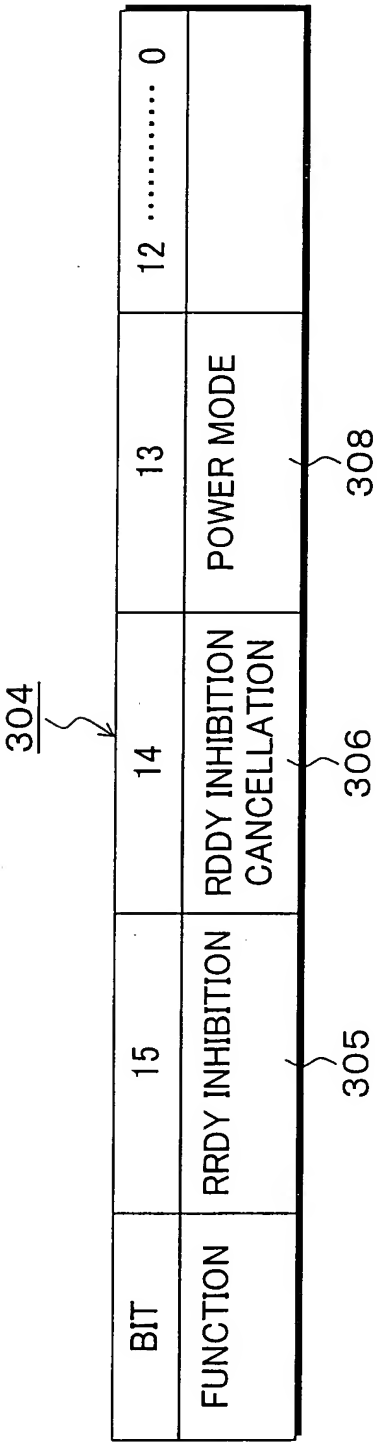

304
BIT
FUNCTION
15
RRDY INHIBITION
14
RDDY INHIBITION CANCELLATION
13
POWER MODE
12 0
305
306
308

FIG. 36A

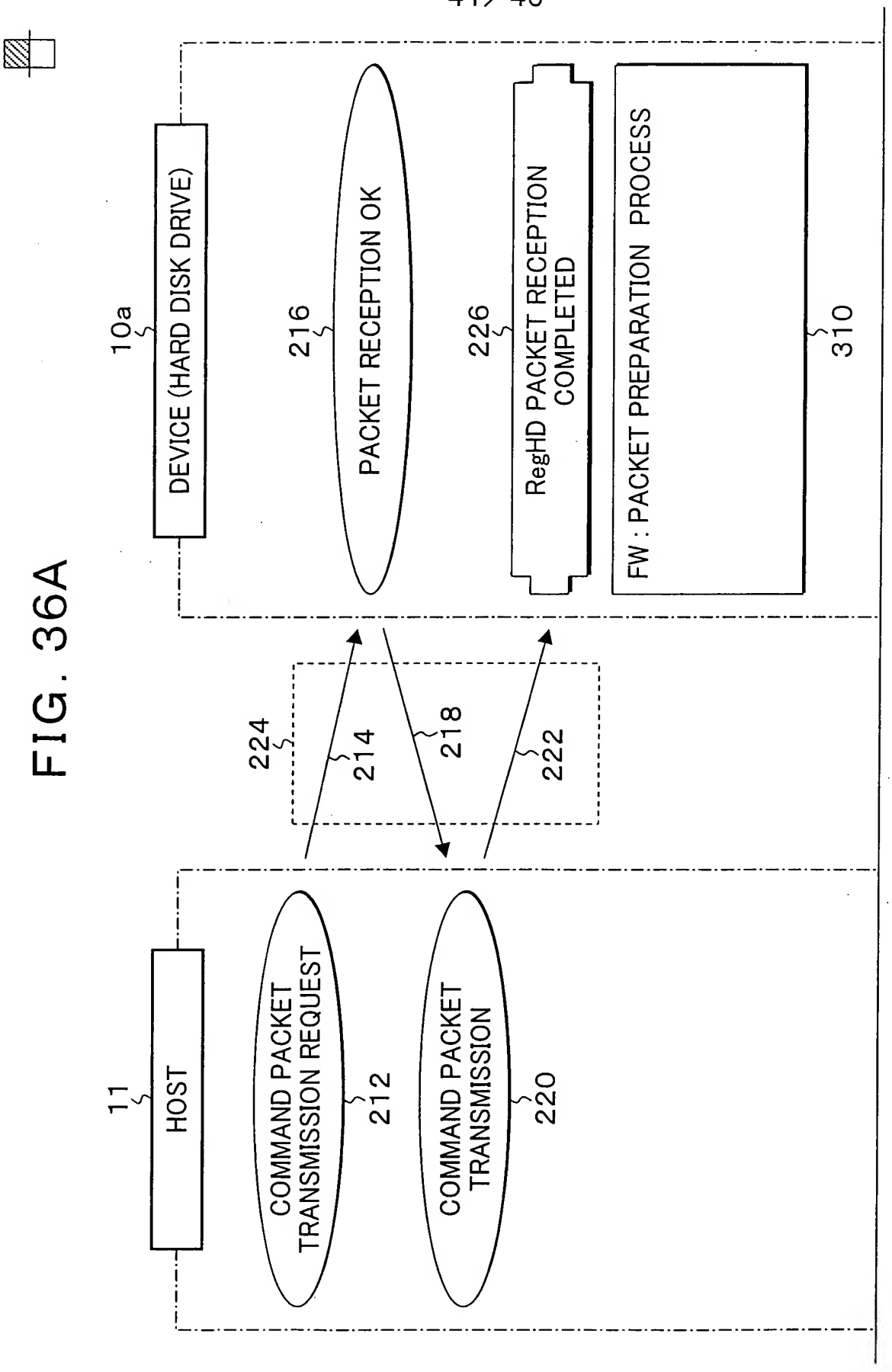

10a
DEVICE (HARD DISK DRIVE)
216
PACKET RECEPTION OK
226
RegHD PACKET RECEPTION COMPLETED
310
FW : PACKET PREPARATION PROCESS
224
214
218
222
11
HOST
COMMAND PACKET TRANSMISSION REQUEST
212
COMMAND PACKET TRANSMISSION
220

FIG. 36B

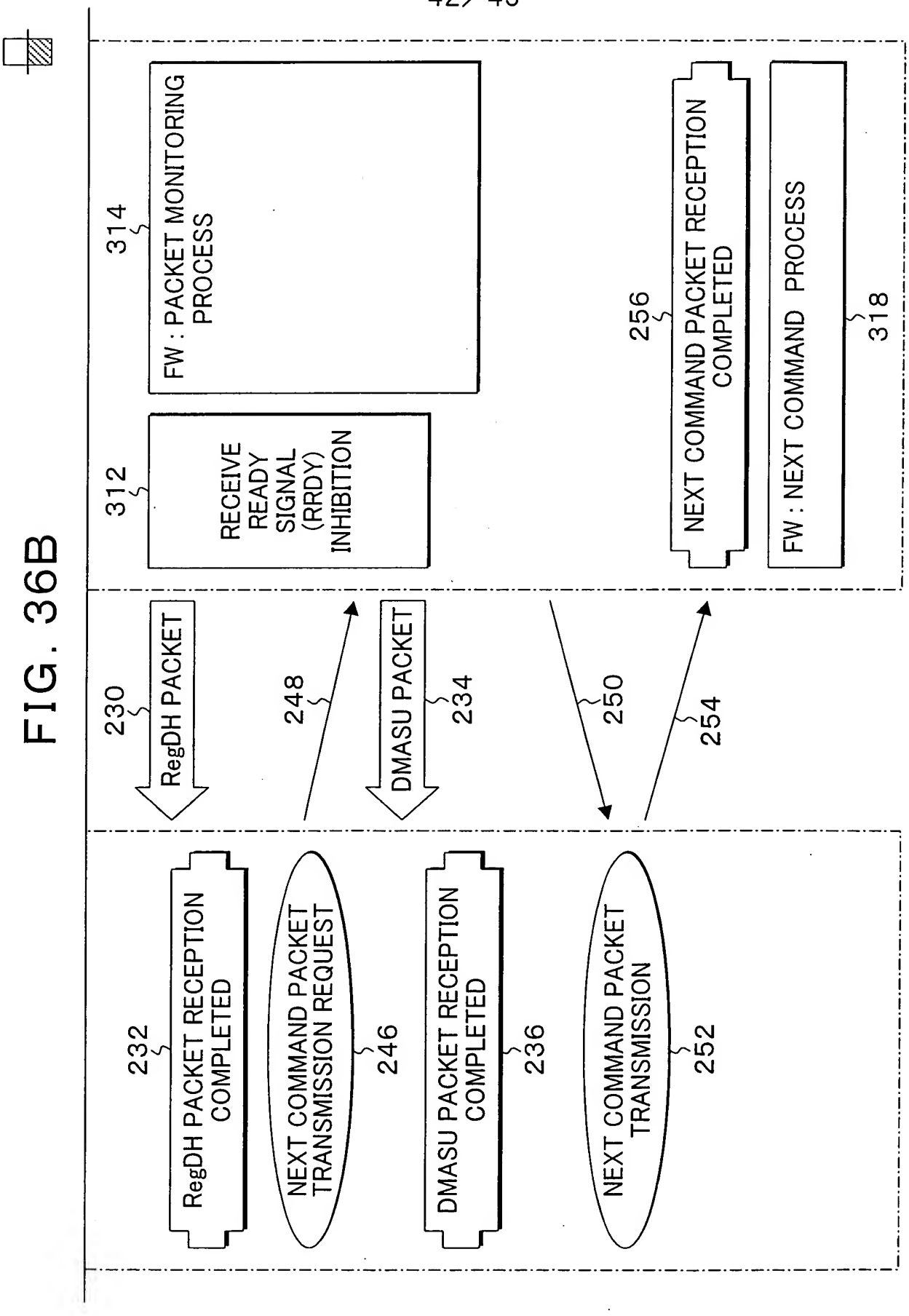

314
FW : PACKET MONITORING PROCESS
312
RECEIVE READY SIGNAL (RRDY) INHIBITION
256
NEXT COMMAND PACKET RECEPTION COMPLETED
318
FW : NEXT COMMAND PROCESS
230
RegDH PACKET
248
DMASU PACKET
234
250
254
232
RegDH PACKET RECEPTION COMPLETED
NEXT COMMAND PACKET TRANSMISSION REQUEST
246
DMASU PACKET RECEPTION COMPLETED
236
NEXT COMMAND PACKET TRANSMISSION
252

FIG. 37

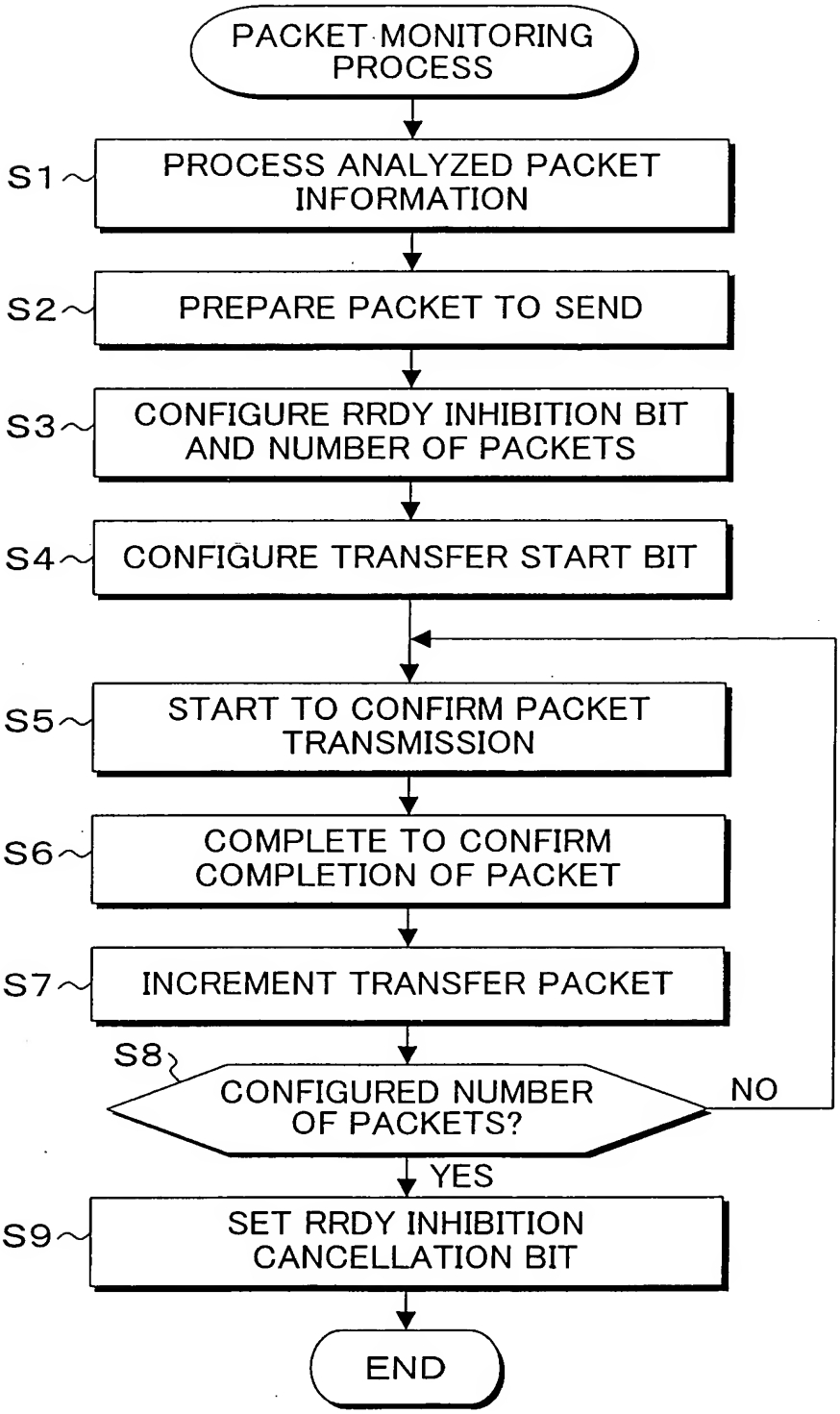

PACKET MONITORING PROCESS
S1
PROCESS ANALYZED PACKET INFORMATION
S2
PREPARE PACKET TO SEND
S3
CONFIGURE RRDY INHIBITION BIT AND NUMBER OF PACKETS
S4
CONFIGURE TRANSFER START BIT
S5
START TO CONFIRM PACKET TRANSMISSION
S6
COMPLETE TO CONFIRM COMPLETION OF PACKET
S7
INCREMENT TRANSFER PACKET
S8
CONFIGURED NUMBER OF PACKETS?
NO
YES
S9
SET RRDY INHIBITION CANCELLATION BIT
END

FIG. 38

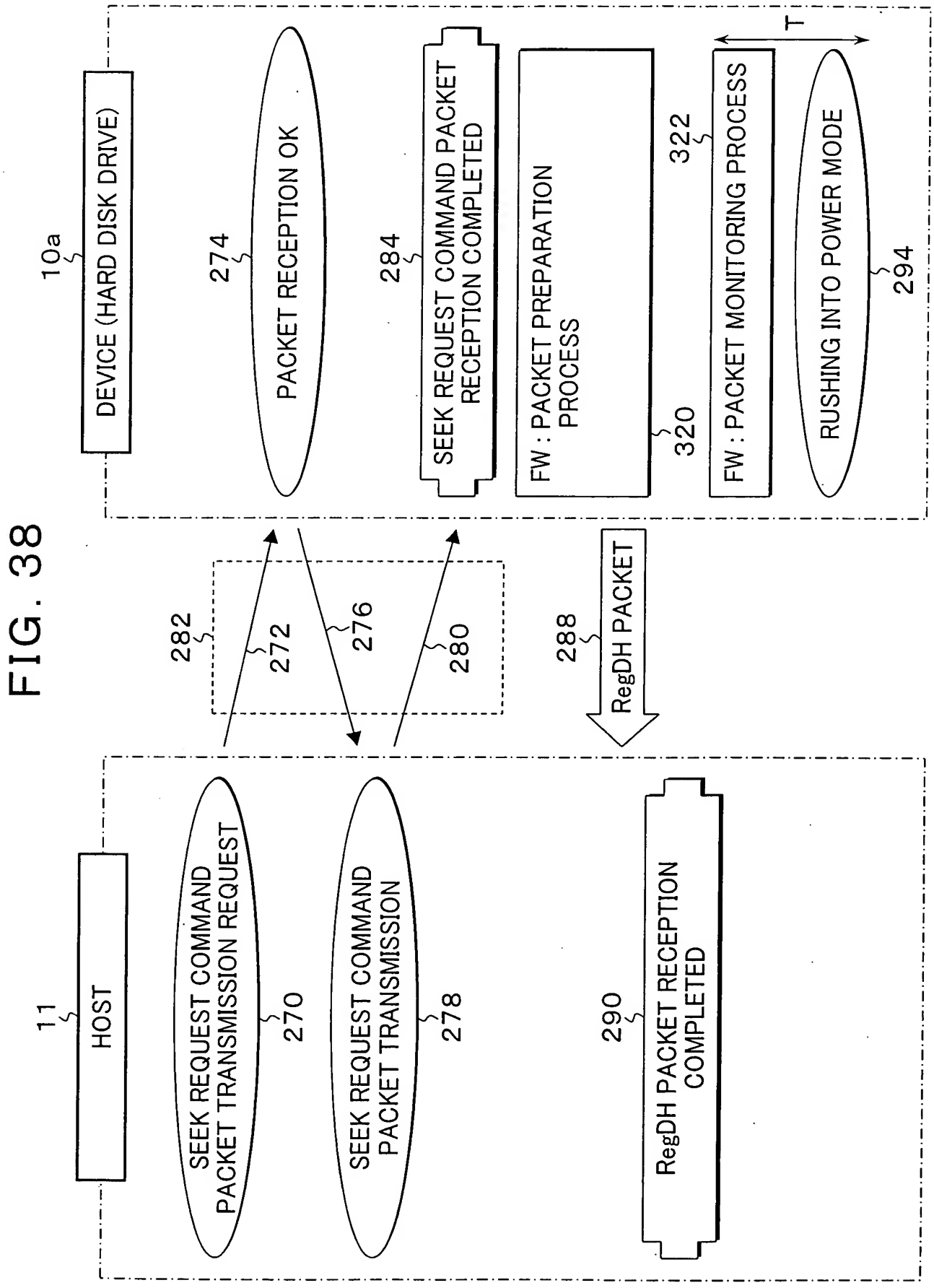
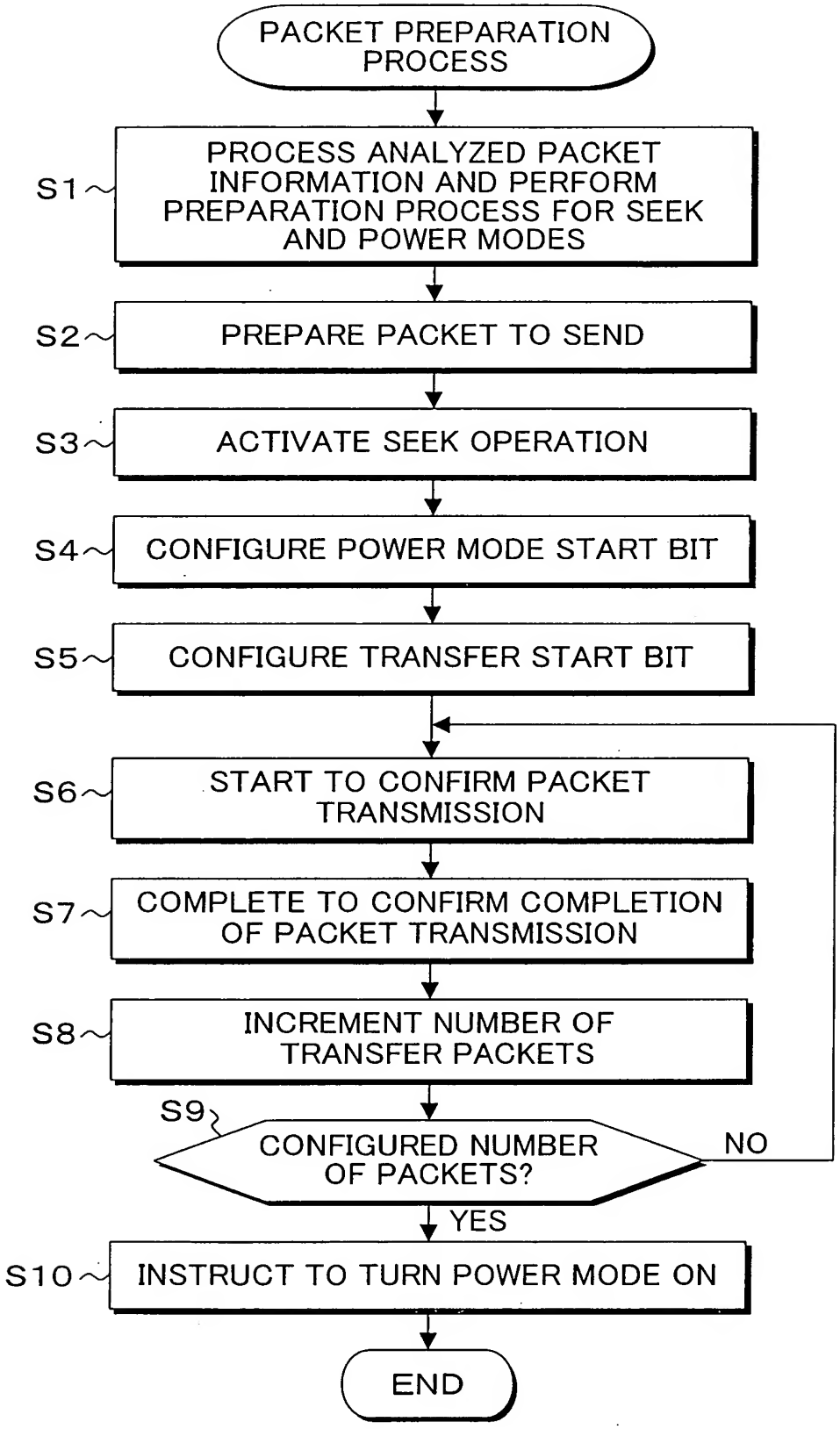

10a
DEVICE (HARD DISK DRIVE)
274
PACKET RECEPTION OK
284
SEEK REQUEST COMMAND PACKET RECEPTION COMPLETED
FW : PACKET PREPARATION PROCESS
320
322
FW : PACKET MONITORING PROCESS
T
RUSHING INTO POWER MODE
294
282
272
276
280
288
RegDH PACKET
11
HOST
SEEK REQUEST COMMAND PACKET TRANSMISSION REQUEST
270
SEEK REQUEST COMMAND PACKET TRANSMISSION
278
290
RegDH PACKET RECEPTION COMPLETED

FIG. 39


PACKET PREPARATION PROCESS
S1
PROCESS ANALYZED PACKET INFORMATION AND PERFORM PREPARATION PROCESS FOR SEEK AND POWER MODES
S2
PREPARE PACKET TO SEND
S3
ACTIVATE SEEK OPERATION
S4
CONFIGURE POWER MODE START BIT
S5
CONFIGURE TRANSFER START BIT
S6
START TO CONFIRM PACKET TRANSMISSION
S7
COMPLETE TO CONFIRM COMPLETION OF PACKET TRANSMISSION
S8
INCREMENT NUMBER OF TRANSFER PACKETS
S9
CONFIGURED NUMBER OF PACKETS?
NO
YES
S10
INSTRUCT TO TURN POWER MODE ON
END